Exhibit 24

National Semiconductor

LVDS MEGABITS @milliwatts

April 25, 1997

Dear Valued Customer:

Enclosed is our first edition of *the LVDS Owner's Manual & Design Guide*. It can be ordered from our Customer Support Centers or through our Website (http://www.national.com) as literature# 550062-001. It can also be downloaded from our Website starting in June. There is a growing trend toward high speed differential serial buses, and this document is intended to help designers become familiar and comfortable with the benefits and use of this important new LVDS technology. The *Owner's Manual* contains:

Chapter 1: "Introduction to LVDS"
Explains how LVDS works and where the standard came from

Chapter 2: "LVDS Advantages"
Includes 3 case studies showing the total cost and performance of LVDS versus other technologies

Chapter 3: "Selecting an LVDS Device"
A selection guide

Chapter 4: "Designing with LVDS"
PCB and other design tips for creating high performance, low noise LVDS applications

Chapter 5: "Cables and Connectors"
Some general guidelines for selecting and using cables and connectors

Chapter 6: "LVDS Evaluation Boards"
A description of available eval boards and instructions for using the Generic LVDS Evaluation Board

Chapters 7 & 8: Reference Information & Index

I hope this and future versions of the *LVDS Owner's Manual* will be of use to you and your co-workers. If you have any questions, please contact your local sales representative or call the Interface Applications Hotline at 408/ 721-8500.

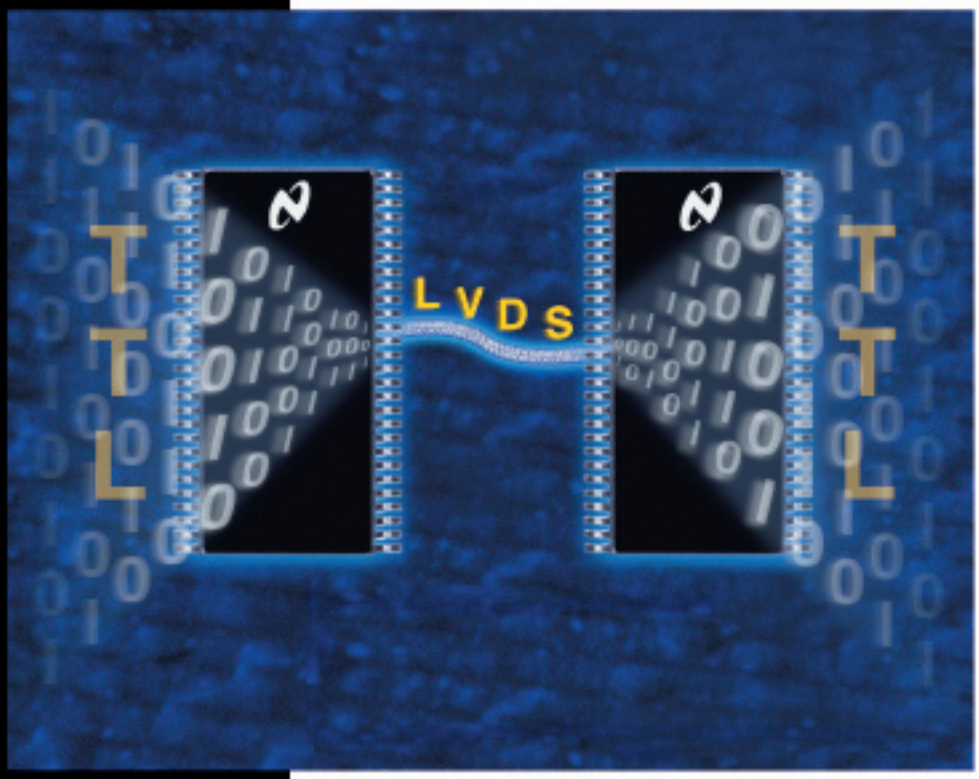
Sincerely,

Interface Signal Management Group
National Semiconductor

EMC EXHIBIT
1019

LVDS OWNER'S MANUAL

SPRING 1997



National Semiconductor

DESIGN GUIDE

Introduction to LVDS

Chapter 1

1.0.0 INTRODUCTION TO LVDS

LVDS stands for Low Voltage Differential Signaling. It is a way to communicate data using a very low voltage swing (about 350mV) over two differential PCB traces or a balanced cable.

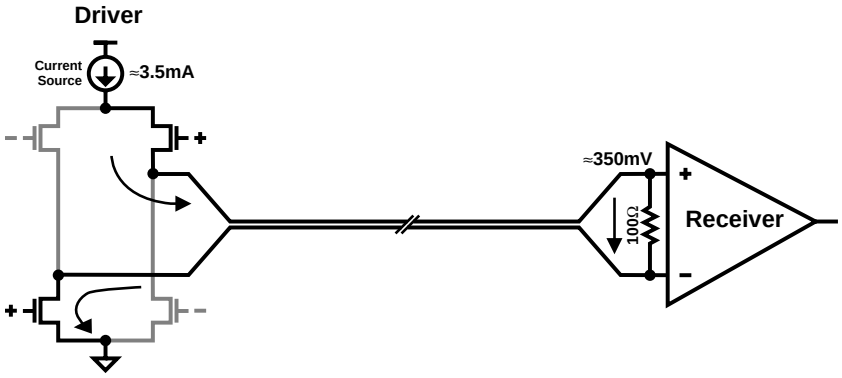
1.1.0 THE TREND TO LVDS

Consumers are demanding more realistic, visual information in the office and in the home. This is driving the need to move video, 3-D graphics, and photorealistic image data from camera to PCs and printers through LAN, phone, and satellite systems to home set top boxes and digital VCRs. Solutions exist today to move this high speed digital data both very short and very long distances: on a printed circuit board (PCB) and across fiber or satellite networks. Moving this data from board to board or box to box, however, requires an extremely high performance solution that consumes a minimum of power, generates little noise (must meet increasingly stringent FCC/CISPR EMI requirements), is relatively immune to noise, and is inexpensive. Unfortunately existing solutions are a compromise of these four basic ingredients: **performance, power, noise, and cost.**

1.2.0 GETTING SPEED WITH LOW NOISE AND LOW POWER

LVDS is a low swing, differential signaling technology which allows single channel data transmission at hundreds of Megabits per second (Mbps). Its low swing and current mode driver outputs create low noise and provide a very low power consumption across frequency.

1.2.1 How LVDS Works



Simplified diagram of LVDS driver and receiver connected via 100Ω controlled differential impedance media.

National's LVDS outputs consist of a current source (nominal 3.5mA) which drives one of the differential pair lines. The receiver has high DC impedance (it does not source or sink DC current), so the majority of driver current flows across the 100Ω termination resistor generating about 350mV across the receiver inputs. When the driver switches, it changes the direction of current flow across the resistor, thereby creating a valid "one" or "zero" logic state.

1.2.2 Why Low Swing Differential?

The differential data transmission method used in LVDS is less susceptible to common-mode noise than single-ended schemes. Differential transmission uses two wires with opposite current/voltage swings instead of the one wire used in single-ended methods to convey data information. The advantage of the differential approach is that noise is coupled onto the two wires as common mode (the noise appears on both lines equally) and is thus rejected by the receivers which looks at only the *difference* between the two signals. The differential signals also tend to radiate less noise than single-ended signals due to the canceling of magnetic fields. And, the current mode driver is not prone to ringing and switching spikes, further reducing noise.

Because differential technologies such as LVDS reduce concerns about noise, they can use lower signal voltage swings. This advantage is crucial, because it is impossible to raise data rates and lower power consumption without using low voltage swings. The low swing nature of the driver means data can be switched very quickly. Since the driver is also current mode, very low — almost flat — power consumption across frequency is achieved since the power consumed by the load (3.5mA x 350mV ≈ 1.2mW) stays almost constant.

1.2.3 The LVDS Standards

Two key industry standards define LVDS: one from the ANSI/TIA/EIA (American National Standards Institute/Telecommunications Industry Association/Electronic Industries Association) and another from the IEEE (Institute for Electrical and Electronics Engineering).

The generic (multi-application) LVDS standard, **ANSI/TIA/EIA-644**, began in the TIA Data Transmission Interface committee TR30.2. The ANSI/TIA/EIA standard defines driver output and receiver input characteristics, thus it is an electrical-only standard. It does not include functional specifications, protocols or even complete cable characteristics since these are application dependent. ANSI/TIA/EIA-644 is intended to be reference by other standards that specify the complete interface (connectors, protocol, etc.). This allows it to be easily adopted into many applications.

ANSI/TIA/EIA-644 (LVDS) Standard

Note: Actual datasheet specifications may be significantly better.

Parameter	Description	Min	Max	Units
V_{OD}	Differential Output Voltage	247	454	mV
V_{OS}	Offset Voltage	1.125	1.375	V
ΔV_{OD}	|Change in V_{OD}|		50	|mV|
ΔV_{OS}	|Change in V_{OS}|		50	|mV|
I_{SC}	|Short Circuit Current|		24	|mA|
t_r/t_f	Output Rise/Fall Times (≥200Mbps)	0.26	1.5	ns
	Output Rise/Fall Times (<200Mbps)		30% of t_{ui}†	
I_{IN}	|Input Current|		20	|µA|
V_{TH}	|Threshold Voltage|		100	|mV|
V_{IN}	Input Voltage Range	0	2.4	V

† t_{ui} is unit interval (i.e bit width).

The ANSI/TIA/EIA standard does specify a recommended maximum data rate of 655Mbps and a theoretical maximum of 1.923Gbps based on a lossless medium. The standard also covers minimum media specifications, fail-safe operation of the receiver under fault conditions, and other configurations issues such as multi-receiver operation. The ANSI/TIA/EIA-644 standard was approved in November 1995. National Semiconductor held the editor position for this standard.

The other LVDS standard is from an IEEE project. This standard came out of an effort to develop a standard for purposes such as linking processors in a multiprocessing system or grouping workstations into a cluster. This Scalable Coherent Interface (SCI) program originally specified a differential ECL interface that provided the high data rates required but did not address power concerns or integration.

The low-power SCI-LVDS standard was later defined as a subset of SCI and is specified in the **IEEE 1596.3** standard. SCI-LVDS specifies also specifies signaling levels (electrical specifications) similar to the ANSI/TIA/EIA-644 standard for the high-speed/low-power SCI physical layer interface. The standard also defines the encoding for packet switching used in SCI data transfers. The IEEE 1596.3 standard was approved in March 1996. National Semiconductor chaired this standardization committee.

In the interest of promoting a wider standard, no specific process technology, medium, or power supply voltages are defined by either standard. This means that LVDS can be implemented in CMOS, GaAs or other applicable technologies, migrate from 5V to 3.3V to sub-3V supplies, and transmit over PCB or cable thereby serving a broad range of applications.

1.2.4 A Quick Comparison

Parameter	RS-422	PECL	LVDS
Differential Driver Output Voltage	±2-5 V	±600-1,000 mV	±250-450 mV
Receiver Input Threshold	±200 mV	±200-300 mV	±100 mV
Data Rate	<30 Mbps	>400 Mbps	>400 Mbps

Parameter (Based on DS90C031/2)	RS-422	PECL	LVDS
Supply Current Quad Driver (no load, static)	60mA	32-65mA (Max.)	3.0mA
Prop. Delay of Driver	11ns (Max.)	4.5ns (Max.)	3.0ns (Max.)
Prop. Delay of Receiver	30ns (Max.)	7.0ns (Max.)	5.0ns (Max.)
Supply Current Quad Receiver (no load, static)	23mA (Max.)	40mA (Max.)	10mA (Max.)
Skew (Driver or Receiver)	N/A	500ps	400ps

The chart above compares LVDS signaling levels with those of PECL and shows that LVDS has half the voltage swing of PECL. LVDS swings are 1/10 of traditional TTL/CMOS and RS-422 levels. Another voltage characteristic of LVDS is that the drivers and receivers do not depend on a specific power supply, such as 5V. Therefore, LVDS has an easy migration path to lower supply voltages such as 3.3V or even 2.5V, while still maintaining the same signaling levels and performance. In contrast, technologies such as ECL or PECL have a greater dependence on the supply voltage, which make it difficult to migrate systems utilizing these technologies to lower supply voltages.

1.2.5 Easy Termination

Whether the LVDS transmission medium consists of a cable or controlled impedance traces on a printed circuit board, the transmission medium must be terminated to its characteristic differential impedance to complete the current loop and terminate high speed signals. If the medium is not properly terminated, signals reflect from the end of the cable or trace and interfere with succeeding signals. Proper termination also reduces unwanted electromagnetic emissions.

To prevent reflections, LVDS requires a terminating resistor of 100Ω ± 20Ω that is matched to the actual cable or PCB traces. This resistor completes the current loop and properly terminates the signal. This resistor is placed across the differential signal lines as close as possible to the receiver input . With this termination, an LVDS driver (DS90C031) can drive a twisted pair wire (e.g. SCSI cable) over 10m at speeds in excess of 155.5Mbps (77.7MHz). The real limitation on speed is two fold: 1) how fast TTL data can be delivered to the driver, 2) bandwidth performance of the selected media (cable). In the case of LVDS drivers like the DS90C031, its speed is limited by how fast the TTL data can be delivered to the driver. (National's Channel Link devices capitalize on the speed mismatch between TTL and LVDS by serializing the TTL data into a narrower LVDS data stream — more about this later.)

The simplicity of the LVDS termination scheme makes it easy to implement in most applications. ECL and PECL can require more complex termination than the one-resistor solution for LVDS. PECL drivers commonly require 220Ω pull down resistors from each driver output, along with 100Ωs across the receiver input.

1.2.6 Saving Power

LVDS technology saves power in several important ways. The power dissipated by the load (the 100Ω termination resistor) is a mere 1.2mW. In comparison, an RS-422 driver typically delivers 3V across a 100Ω termination, for 90mW power consumption — 75 times more than LVDS. Similarly, LVDS devices require roughly one-tenth the power supply current of PECL/ECL devices.

Aside from the power dissipated in the load and static I_{CC} current, LVDS also lowers system power through its CMOS current-mode driver design. This design greatly reduces the frequency component of I_{CC}. The I_{CC} vs. Frequency plot for LVDS is virtually flat between 10MHz and 100MHz for the quad devices (<50mA total for driver+receiver at 100MHz). Compare this to TTL/CMOS transceivers whose dynamic power consumption increases exponentially with frequency.

1.2.7 Fail-Safe Feature

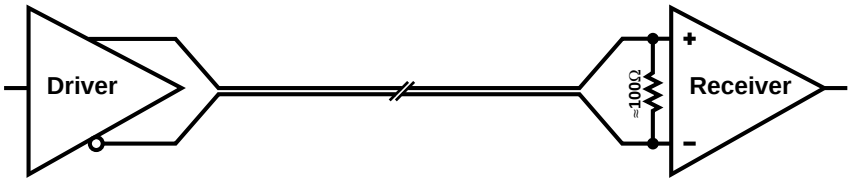
To help ensure reliability, LVDS receivers have a fail-safe feature that guarantees the output to be in a known logic state (HIGH) under certain fault conditions. These conditions include open, shorted, or terminated receiver inputs.

If the driver loses power, is disabled or is removed from the line, while the receiver stays powered on with inputs terminated, the receiver output remains in a known state with the fail-safe feature.

If LVDS receivers did not have the fail-safe feature and one of the fault conditions occurred, any external noise above the receiver thresholds could trigger the output and cause an error. A receiver without fail-safe could even go into oscillation under certain fault conditions. The fail-safe features ensures that the receiver output will be a HIGH — rather than an unknown state — under fault conditions.

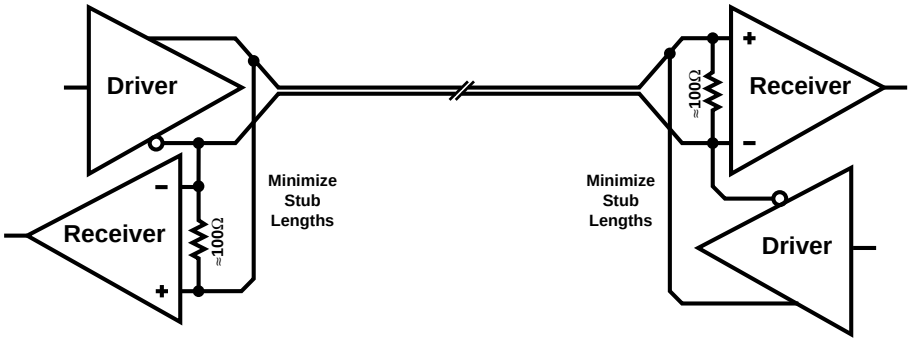
With the fault conditions accommodated internal to the receiver, designers do not need to include the external biasing resistors required by other technologies. This LVDS advantage saves valuable board space, cost, and design headaches.

1.2.8 LVDS Configurations

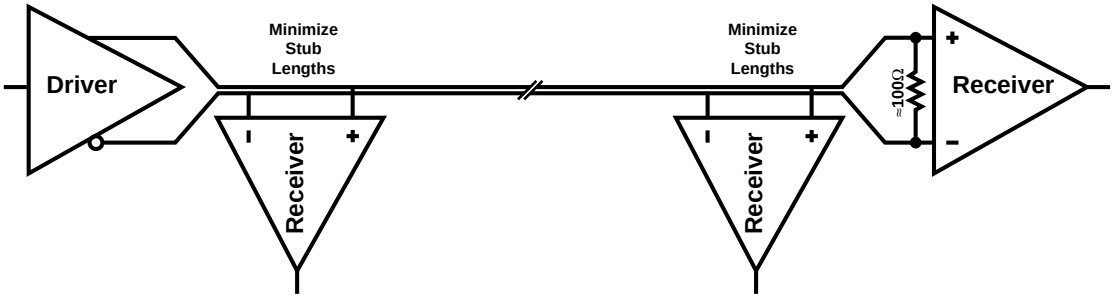


Point-to-point configuration.

Although LVDS drivers and receivers are typically used in a point-to-point arrangement (above), other topologies are possible. The configuration shown next allows bi-directional communication over a single twisted pair. Data can flow in only one direction at a time. The requirement for two terminating resistors reduces the signal (and thus the differential noise margin), so this configuration should be considered only where noise is low and transmission distance is short (≤10m).



Bi-directional half-duplex configuration.



Multidrop configuration.

A multidrop configuration can also be used if transmission distance is short and stub lengths are less than 12mm (<7mm is recommended). Dedicated point-to-point links are still the preferred solution. LVDS has many advantages that make it likely to become the next data transmission standard for data rates at and above 100Mbps for distances around 10m or less. In this role, LVDS will far exceed the 20Kbps to 30Mbps rates of the RS-232, RS-422, and RS-485 standards.

1.3.0 SAVE MONEY TOO

LVDS can save money in several important ways:

1) National's LVDS solutions are inexpensive CMOS implementations.

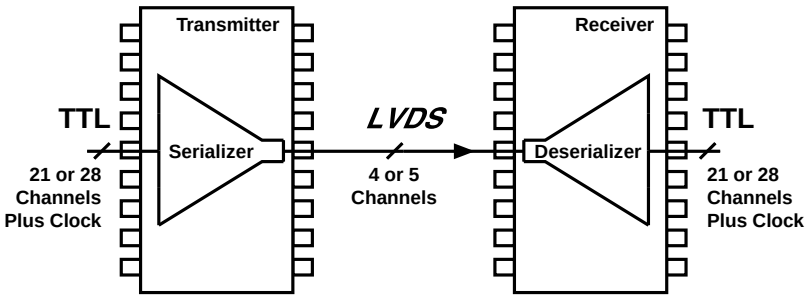
2) High performance can be achieved using low cost, off-the-shelf CAT3 cable and connectors.

3) LVDS consumes very little power, so power supplies, fans, etc. can be reduced or eliminated.

4) LVDS is a low noise producing, noise tolerant technology power supply and EMI noise headaches are greatly minimized.

5) LVDS transceivers are relatively inexpensive and can also be integrated around digital cores.

6) Since LVDS can move data so much faster than TTL, multiple TTL signals can be serialized or muxed into a single LVDS channel, reducing board, connector, and cable costs. National's family of Channel Link devices do just that. A channel link transmitter takes 21 or 28 bits of TTL data and converts it to 4 or 5 LVDS channels. These 4 or 5 channels of LVDS can then be routed across controlled impedance PCB traces or cable to the receiver which converts the data back to TTL.



National's Channel Link chipsets convert a TTL bus into a compact LVDS data stream and then back to TTL.

The conversion of a wide TTL bus to a few LVDS channels using Channel Link can substantially lower the power required to move the data, reduce noise and EMI concerns, and dramatically cut the size and number of PCB layers, connector pins, and cable conductors. In fact in most cases, the PCB, cable, and connector cost savings greatly overshadow any additional silicon costs. Smaller PCBs, cables, and connectors also result in a much more ergonomic (user-friendly) system.

1.4.0 LVDS APPLICATIONS

The high speed and low power/noise/cost benefits of LVDS broaden the scope of LVDS applications far beyond those for traditional technologies. Here are some examples:

PC/Computing	Telecom/Datacom	Consumer/Commercial
Flat panel displays	Switches	Home/commercial video links
Monitor link	Add/drop multiplexers	Set top boxes
SCI processor interconnect	Hubs	In-flight entertainment
Printer engine links	Routers	Game displays/controls
Digital Copiers		
System clustering	(Box-to-box & rack-to-rack)	
Multimedia peripheral links		

1.5.0 NATIONAL'S WIDE RANGE OF LVDS SOLUTIONS

National Semiconductor offers LVDS technology in several forms. For example, National's 5V DS90C031/DS90C032 and 3V DS90LV031/DS90LV032 quad line driver/receiver devices implement LVDS technology in discrete packages for general-purpose use. This family of basic line drivers and receivers also contains singles, duals and transceivers.

For the specialized task of connecting laptop and notebook computers to their high-resolution LCD screens, National offers the Flat Panel Display Link (FPD-Link) LVDS interface devices. These parts make it practical for portable computers to take advantage of the same high screen resolutions used in CRT-based desktop PCs.

Another more generalized use of LVDS is in the National Channel Link family which can take 21 or 28-bits of TTL data and convert it to 3 or 4 channels of LVDS plus clock. These devices provide fast data pipes (up to 1.84Gbps throughput) and are well suited for high-speed network hubs or routers applications or anywhere a low cost high speed link is needed. Their serializing nature provides an overall savings to system cost as cable and connector physical size and cost are greatly reduced.

1.6.0 CONCLUSION

National's LVDS technology solutions eliminate the trade-offs in speed, power, noise, and cost for high performance data transmission applications. In doing so, LVDS not only achieves great benefits in existing applications, but opens the door to many new ones.

LVDS Advantages

Chapter 2

2.0.0 LVDS ADVANTAGES

2.1.0 LVDS ELECTRICAL CHARACTERISTICS

LVDS current-mode, low-swing outputs mean that LVDS can drive at high speeds (up to several hundred Mbps over short distances). If high speed differential design techniques are used, signal noise and electromagnetic interference (EMI) can also be reduced with LVDS because of:

1) The low output voltage swing (≈350mV)

2) Relatively slow edge rates, dV/dt ≈ 0.350V/0.5ns = 0.7V/ns

3) Differential (odd mode operation) so magnetic fields tend to cancel

4) "Soft" output corner transitions

5) Minimum I_{CC} spikes due to low current mode operation

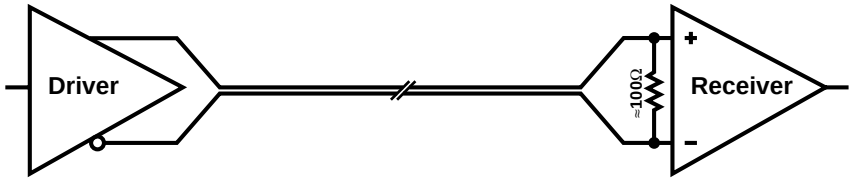
LVDS can be designed using CMOS processes, allowing LVDS to be integrated with standard ASICs. LVDS can be used in commercial, industrial, and even military temperature ranges and operate from power supplies down to 2 volts. LVDS uses common copper PCB traces and readily available cables and connectors as transmission media, unlike fiber optics.

Presently the major limitations of LVDS are its point-to-point nature (as opposed to multipoint) and short transmission distance (10-15m), where other technologies must presently be used.

Advantages	LVDS	PECL	Optics	RS-422	GTL	TTL
Data rate up to 1Gbps	+	+	+	-	-	-
Very low skew	+	+	+	-	+	-
Low dynamic power	+	-	+	-	-	-
Cost effective	+	-	-	+	+	+
Low noise/EMI	+	+	+	-	-	-
Single power supply/reference	+	-	+	+	-	+
Migration path to low voltage	+	-	+	-	+	+
Simple termination	+	-	-	+	-	+
Wide common mode range	-	+	+	+	-	-
Process independent	+	-	+	+	+	+
Allows integration w/digital	+	-	-	-	+	+
Cable breakage/splicing issues	+	+	-	+	+	+
Long distance transmission	-	+	+	+	-	-
Industrial temp/voltage range	+	+	+	+	+	+

2.2.0 LVDS DRIVERS & RECEIVERS

The most basic LVDS devices are the driver and receiver. These translate TTL to LVDS and back to TTL.

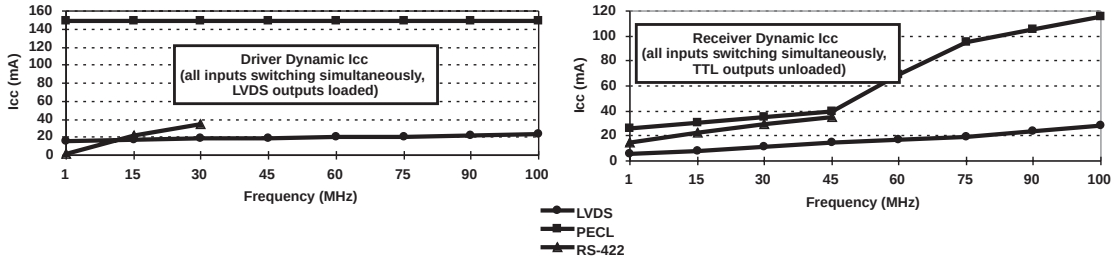


LVDS drivers and receivers convert TTL to LVDS and back to TTL.

Drivers and receivers transmit high speed data across distances up to 10m at very low power, noise, and cost.

Parameter	LVDS	PECL	Optics	RS-422	GTL	TTL
Output voltage swing	±350mV	±800mV	n/a	±2-5V	1.2V	2.4-5V
Receiver threshold	±100mV	±200mV	n/a	±200mV	100mV	1.2V
Speed (Mbps)	>400	>400	1000	<30	<200	<100
Dynamic power	Low	High	Low	Low	High	High
Noise	Low	Low	Low	Low	Med	High
Cost	Low	High	High	Low	Low	Low

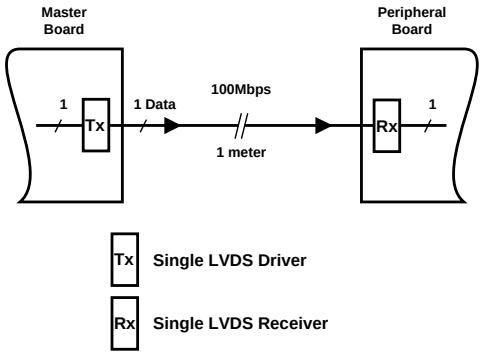
The table above summarizes that only LVDS can deliver the high speed, ultra-low power, and low cost without compromise. PECL and ECL are expensive and consume too much power. TTL/CMOS is cheap, but is noisy and burns a lot of power at high speeds. Fiber optics are expensive and have cables and connectors which are hard to manage.



I_{CC} vs. Frequency for 5V DS90C031/032 LVDS, 41LG/LF PECL, and 26C31/32 RS-422 devices.

2.2.1 100Mbps Serial Interconnect

LVDS drivers and receivers are generally used to create serial or pseudo-serial point-to-point interconnects from 1Mbps to 400Mbps per channel. The following example summarizes the total performance and cost advantages of using LVDS over PECL or TTL for a serial 100Mbps 1 meter point-to-point link. Significantly higher data rates can be achieved for LVDS and PECL.



100Mbps Board-to-Board Link

100Mbps Serial Bitstream

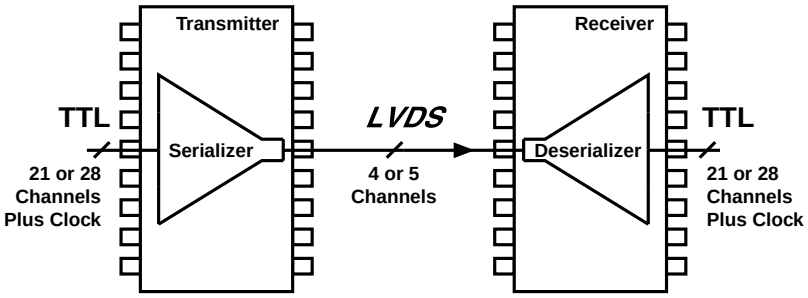
Performance Estimate				
Characteristic	**Parameter**	**LVDS**	**TTL**	**PECL**
Speed	Application Data Rate (Mbps)	100	100	100
	Max Capability per Channel (Mbps)	200	100	200
Power Consumption	Dynamic (mA) (@ 50MHz)	Low	High	Medium
	Static (mA)	8	10	48
Noise	Low EMI	+++	- - -	++
	Low Bounce	+++	- - -	++
Relative System Cost	**Total**	**4.05**	**3.30**	**6.10**
Cost Estimate				
Subsystem	**Parameter**	**LVDS**	**TTL**	**PECL**
General	Single-Ended or Differential	Differential	Single-Ended	Differential
	TTL Bus Width	1	1	1
	TTL Bus Speed (MHz)	50	50	50
	# Master Boards	1	1	1
	# Slave Boards	1	1	1
Transceivers	Description	DS90LV017/018	74LVT125	10ELT20/21
	# Drivers/Board (Master Board)	1	1	1
	# Rec/Board (Peripheral Board)	1	1	1
	Unit Cost	1.00	0.60	2.00
	Silicon Cost per Board	2.00	1.20	4.00
Termination	Voltage	None	None	None
	# Termination Regulators	0	0	0
	Unit Cost	0.00	0.00	0
	# Termination Resistors	1	2	2
	Unit Cost	0.05	0.05	0.05
	# Termination Capacitors	0	0	0
	Unit Cost	0.00	0.00	0.00
	Total Termination Cost	0.05	0.10	0.10
Transmission Medium	Cable Type	2 Pair CAT3	2 Pair CAT3	2 Pair CAT3
	Distance	1m	1m	1m
	#Conductors	2	2	2
	#Cables	1	1	1
	Connector Type	4-pin Wire to Board	4-pin Wire to Board	4-pin Wire to Board
	Unit Cable+Connector Assembly Cost	2.00	2.00	2.00
	Total Media Cost	2.00	2.00	2.00
Total Relative System Cost		**4.05**	**3.30**	**6.10**

Total Performance and Cost Estimates

The preceding example shows that LVDS provides a high speed link with minimal noise, power, and cost. LVDS also creates an easy migration path to higher speeds, lower supply voltages, and higher integration that the other do not.

2.3.0 LVDS CHANNEL LINK SERIALIZERS

The speed of the LVDS line drivers and receivers is limited by how fast the TTL signals can be switched. Therefore, National has introduced a family of Channel Link serializers and deserializers. Instead of using one LVDS channel for every TTL channel, the Channel Link devices send multiple TTL channels through every LVDS channel thereby matching the speed of LVDS to that of TTL.



National's Channel Link serializers/deserializers can dramatically reduce the size (and cost) of cables and connectors.

Using fewer channels to convey data also means power and noise can be lower. The biggest advantage, however, is the significant reduction of cable and connector size. Since cables and connectors are usually quite expensive compared to silicon, dramatic cost savings can be achieved. Channel Link chipsets reduce cable size by up to 80%, reducing cable costs by as much as 50%. Plus, smaller cables are more flexible and user-friendly.

LVDS Channel Link serializer/deserializer devices take the inherent high speed low power, noise, and cost advantages of LVDS and capitalize on the slow speed of TTL to generate significant benefits. For a small increase in silicon cost, Channel Link products can dramatically reduce total system costs and improve total system performance. Therefore, the total system should be evaluated if the true advantages are to be quantified. The following sections summarizes the cost and performance benefits of using Channel Link devices.

2.2.1 1Gbps 16-bit Interconnect

National's Channel Link serializers/deserializers take the benefits of LVDS (high speed and low power, noise, and cost) and add serialization to further reduce cable, connector, and PCB size and cost. Channel Link is a great solution for high speed data bus extension when the the overhead of protocols is not desired. The following example compares the total performance and cost of moving a 16-bit 66MHz bus across 1 meter of cable using the 3V 66MHz 21-bit DS90CR215/216 Channel Link devices versus other solutions.

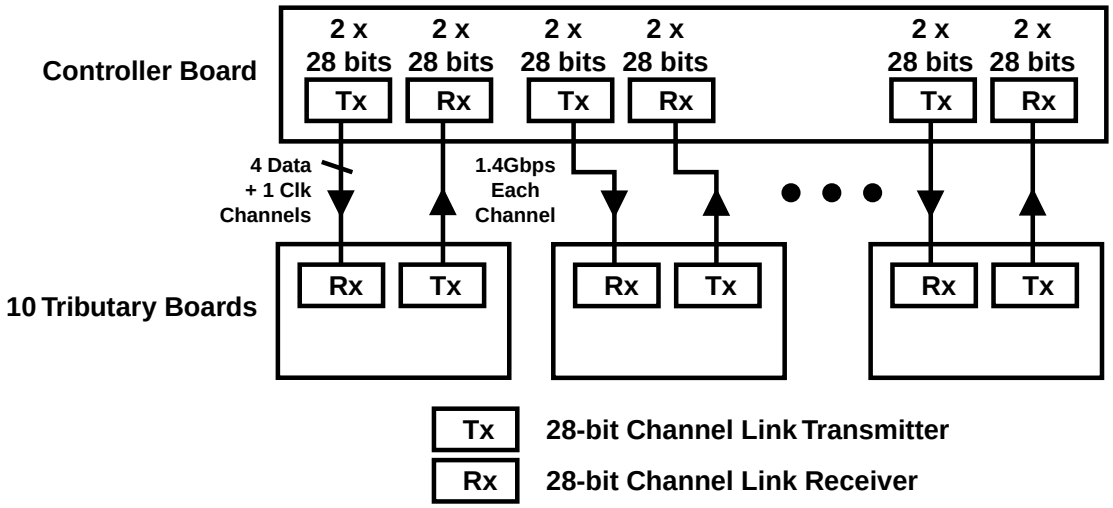
16-Bit Cable Interconnect

Performance Estimate						
Characteristic	**Parameter**	**Channel Link**	**TTL**	**GTL**	**ECL**	**Fibre Channel**
Speed	Application Data Rate (Mbps)	1056	1056	1056	1056	1056
	Max Capability per Channel (Mbps)	462	100	150	800	800
Power Consumption	Dynamic (mA) (@ 66MHz)	180	300	500	300	?
	Static (mA) (Outputs Disabled)	0.02 (Power Dn)	1	50	50	135
Noise	Low EMI	+++	- - -	- -	+	+++
	Low Bounce	+++	- - -	- -	++	+++
Ergonomics	Compact System Size	+++	- -	- -	- - -	+++
	Compact Transmission Medium Size	+++	-	+	+	+++
	Low Weight	+++	-	-	-	+++
Relative System Cost	**Total**	**25.50**	**55.80**	**58.80**	**71.80**	**77.60**
Cost Estimate						
Subsystem	**Parameter**	**Channel Link**	**TTL**	**GTL**	**ECL**	**Fibre Channel**
General	Single-Ended or Differential	Differential	Single-Ended	Single-Ended	Differential	Differential ECL
	TTL Bus Width	16	16	16	16	16
	TTL Bus Speed (MHz)	66	66	66	66	66
	Multiplexed Scheme?	Yes	No	No	No	Yes
	# Master Boards	1	1	1	1	1
	# Slave Boards	1	1	1	1	1
Transceivers	Description	3V 21:4 Channel Link	ALVT 16-Bit	GTL 18-Bit	9-Bit Translators	Fibre Channel
	# Drivers/Board (Master Board)	1	1	1	2	1
	# Rec/Board (Peripheral Board)	1	1	1	2	1
	Unit Cost	5.00	2.50	3.50	5.00	20.00
	Silicon Cost per Board	10.00	5.00	7.00	20.00	40.00
PC Board	Layers	4	12	12	12	12
	Size (Normalized)	1.15	1	1.15	15.63	11.97
	Total Additional PCB Cost	0.00	15.00	15.00	15.00	15.00
Termination	Voltage	None	None	1.5V	2.1V	3.0V
	# Termination Regulators	0	0	1	1	1
	Unit Cost	0.00	0.00	1.00	1.00	1.00
	# Termination Resistors	10	16	16	16	32
	Unit Cost	0.05	0.05	0.05	0.05	0.05
	# Termination Capacitors	0	0	0	0	0
	Unit Cost	0.00	0.00	0.00	0.00	0.00
	Total Termination Cost	0.50	0.80	1.80	1.80	2.60
Transmission Medium	Cable Type	SCSI2 CAT3 Cable	Shielded Flat Cable	Shielded Flat Cable	SCSI2 CAT3 Cable	CAT5 Cable
	Distance	2m	2m	2m	2m	2m
	#Data+Clock Conductors	8	17	17	34	2
	#Power+Ground Conductors	4	10	10	15	2
	#Cables	1	1	1	1	1
	Connector Type	0.050 D - 20	D - 37	D - 37	0.050 D - 50	DB-9
	Unit Cable+Connector Assembly Cost	20.00	30.00	30.00	30.00	15.00
	Total Media Cost	15.00	30.00	30.00	30.00	15.00
Power Supply	Special Supply Voltages	0	0	1.5V	2.1V	3.0V
	Power Supply Size (Normalized)	1	1.3	1.2	1.2	1.2
	Total Add'l Power Supply Cost	0.00	5.00	5.00	5.00	5.00
Total Relative System Cost		**25.50**	**55.80**	**58.80**	**71.80**	**77.60**

Total Performance and Cost Estimates

2.2.2 1.4Gbps 56-Bit Backplane

In some large datacom and telecom systems, it is necessary to construct a very large, high speed backplane. There is generally an inverse relationship between the size of a backplane and its maximum speed. In other words, if you try to make a backplane too large, the heavy loading will severely hamper backplane speed and make power and noise a big problem. Therefore, connecting or extending smaller backplanes via a high speed cable interconnect is often the only solution. The previous examples illustrates how Channel Link may be used to accomplish this over cable. The cost benefits of using Channel Link to shrink cable and connector costs are clear. What would happen, however, if Channel Link were used to form or extend a backplane using a PCB as the medium. The following examples shows how Channel Link can reduce the size and number of layers of the printed circuit board transmission medium in the same way as Channel Link reduces the size and cost of cables.



1.4Gbps Backplane Using Point-to-Point Channel Links

56-Bit Blackplane

Performance Estimate						
Characteristic	**Parameter**	**Channel Link**	**TTL**	**GTL/BTL**	**ECL**	**Fibre Channel**
Speed	Application Data Rate (Mbps)	1400	1400	1400	1400	1400
	Max Capability per Channel (Mbps)	462	100	150	800	800
Power Consumption	Dynamic (mA) (@ 50MHz)	2600	10000	6000	16000	?
(Loaded Tx/Rx's only)	Static (mA)	0.4 (Power on)	40	1840	3402	3818
Noise	Low EMI	+++	---	+	+	++
	Low Bounce	+++	---	+	+	++
Ergonomics	Compact System Size	++	+	+	+	++
	Compact Transmission Medium Size	++	-	+	+	++
	Fans?	No	No	No	Yes	Yes
	Low Weight	+++	-	-	-	+++
Relative System	**Cost Per Board**	**51.05**	**66.12**	**75.04**	**191.04**	**574.22**
	Total	**510.50**	**661.20**	**750.40**	**1910.40**	**5742.20**
Cost Estimate						
Subsystem	**Parameter**	**Channel Link**	**TTL**	**GTL/BTL**	**ECL**	**Fibre Channel**
General	Single-Ended or Differential	Differential	Single-Ended	Single-Ended	Single-Ended	Differential
	TTL Bus Width	56	56	56	56	56
	TTL Bus Speed (MHz)	50	50	50	50	50
	Multiplexed Scheme?	Yes	No	No	No	Yes
	Number Tributary Boards	10	10	10	10	10
	Number Channels in Link	10	56	56	56	14
	Number Conductors (Data)	20	56	56	56	28
	Number Conductors (CLK)	1	1	1	1	1
Transceivers	Description	28:5 Channel Link	LVT 16-Bit	GTL 18-Bit	9-Bit	Fibre Channel
	# Transceivers/Board (Trib Board)	4	4	4	14	14
	# Transceivers/Board (Ctrlr Board)	4	4	4	14	14
	Unit Cost	6.00	2.50	3.50	5.00	20.00
	Silicon Cost per Board	48.00	20.00	28.00	140.00	560.00
PC Board	Layers	12	26	26	26	12
	Size (Normalized)	1.15	1	1.15	15.63	11.97
	Total Additional PCB Cost	0.00	100.00	100.00	150.00	50.00
Termination	Voltage	None	None	1.5V	2.1V	3.0V
	Number Termination Regulators	0	0	14	14	14
	Unit Cost	0.00	0.00	1.00	1.00	1.00
	Number Termination Resistors	10	224	128	128	14
	Unit Cost	0.05	0.05	0.05	0.05	0.05
	Number Termination Capacitors	0	0	0	0	0
	Unit Cost	0.00	0.00	0.00	0.00	0.00
	Total Termination Cost	0.50	11.20	20.40	20.40	14.70
Transmission Medium	Type	PCB Trace Backplane	PCB Trace Backplane	PCB Trace Backplane	PCB Trace Backplane	PCB Trace Backplane
	Distance	<1m	<1m	<1m	<1m	<1m
	Layers	12	26	26	26	12
	Size (Normalized)	1	1	1	1	1
	Number Media	1	1	1	1	1
	Additional Media Cost	0.00	200.00	200.00	200.00	0.00
	Total Add'l Trans. Media Cost	0.00	200.00	200.00	200.00	0.00
Connectors	Connector Type	Header	VME	VME	VME	Header
	Number Pins (Data+ CLK)	21	57	57	57	29
	Number Pins (Power/GND)	5	38	38	7	7
	Total Connector Pins	26	96	96	64	36
	Number Connector Pairs	1	1	1	1	1
	Cost of Pair	3.00	10.00	10.00	8.00	3.75
	Connector Cost per Board	3.00	10.00	10.00	8.00	3.75
Power Supply	Special Supply Voltages	0	0	1.5V	2.1V	3.0V
	Power Supply Size (Normalized)	1	1.5	1.5	1.7	1.4
	Total Add'l Power Supply Cost	0.00	50.00	50.00	60.00	40.00
Total Relative System Cost Per Board		**51.05**	**66.12**	**75.04**	**191.04**	**574.22**
Total Relative System Cost		**510.50**	**661.20**	**750.40**	**1910.40**	**5742.20**

Total Performance and Cost Estimates

Selecting an LVDS Device

Chapter 3

3.0.0 SELECTING AN LVDS DEVICE

3.1.0 GENERAL

National is continually expanding its portfolio of LVDS devices. The devices listed below are current at the time this book goes to press. For the latest list of LVDS devices, contact your local National Semiconductor representative (listed on the back cover of this book). By far the best way to acquire the latest LVDS datasheet is through National's Website: http://www.national.com. The Web is constantly updated with new documents, whereas databooks and datasheets are printed infrequently. Applications questions should be directed to your local National Semiconductor representative or to the US National Interface Hotline: 1-408-721-8500 (8am to 5pm PST).

3.2.0 LVDS LINE DRIVERS & RECEIVERS

LVDS line drivers and receivers are used to convey information over PCB trace or cable if, (1) you only have a few channels of information to transmit, or (2) your data is already serialized. The table below summarizes National's LVDS line drivers and receivers.

LVDS Driver/Receiver Solutions

Order Number	Number of Drivers	Number of Receivers	Power Supply	Temp Range	Data Rate	Approx. I_{CC} @ 1Mbps	Max I_{CC} Disabled	Max Driver Prop Delay	Max Driver Channel Skew	Max Receiver Prop Delay	Max Receiver Channel Skew	Package	Comments	Eval Board Lit #
DS90C031TM	4	0	5	Ind	>155Mbps	21	4	3.5	1.0	—	—	16 SOIC	Ganged Enable	550061-001
DS90C031E-QML	4	0	5	Mil	>100Mbps	25	10	5.0	3.0	—	—	20 LCC	Military -883	550061-001
DS90C032TM	0	4	5	Ind	>155Mbps	11	10	—	—	6.0	1.5	16 SOIC	Ganged Enable	550061-001
DS90C032E-QML	0	4	5	Mil	>100Mbps	11	11	—	—	8.0	3.0	20 LCC	Military -883	550061-001
DS36C200M	2	2	5	Com	>155Mbps	17	10	5.5	—	9.0	—	16 SOIC	1394 Link	–
DS90C401M	2	0	5	Com	>155Mbps	21	6.5	3.5	1.0	—	—	8 SOIC		550061-001
DS90C402M	0	2	5	Com	>155Mbps	11	10	—	—	6.0	1.5	8 SOIC		550061-001
DS90LV031TM	4	0	3.3	Ind	>100Mbps	19	3	5.0	1.8	—	—	16 SOIC	Ganged Enable	550061-001
DS90LV032TM	0	4	3.3	Ind	>100Mbps	19	15	—	—	6.5	1.7	16 SOIC	Ganged Enable	550061-001
DS90LV017M	1	0	3.3	Com	>100Mbps	4	7	6.0	—	—	—	8 SOIC		550061-001
DS90LV027M	2	0	3.3	Com	>100Mbps	TBD	7	6.0	TBD	—	—	8 SOIC		550061-001
DS90LV018M	0	1	3.3	Com	>200Mbps	TBD	TBD	—	—	TBD	—	8 SOIC	Fall 1997	550061-001
DS90LV028M	0	2	3.3	Com	>200Mbps	TBD	TBD	—	—	TBD	TBD	8 SOIC	Fall 1997	550061-001
DS90LV019TM	1	1	3.3/5	Ind	>155Mbps	TBD	6	3.5	—	6.0	—	14 SOIC	Summer 1997	–
DS90LV031ATM	4	0	3.3	Ind	400Mbps	3.5	5	2.5	0.5	—	—	16 SOIC	Fall 1997	550061-001
DS90LV032ATM	0	4	3.3	Ind	400Mbps	1.5	15	—	—	3.5	0.5	16 SOIC	Fall 1997	550061-001

Note: When using drivers/receivers to transmit clock signals, multiply the clock frequency by 2 to get data rate.
Thus, a 50 MHz clock has 2-bits of information (a high bit and a low bit) for every clock period resulting in a 100 Mbps signal.

3.3.0 LVDS CHANNEL LINK SERIALIZERS/DESERIALIZERS

If you have a wide TTL bus that you wish to transmit, use one of National's Channel Link devices. Channel Link will serialize your data for you, saving you money on cables and connectors and helping you avoid complex skew problems associated with a completely parallel solution. The next table summarizes National's Channel Link devices.

Channel Link Solutions

Order Number	Mux/ Demux Ratio	Transmitter/ Receiver	Power Supply	Clock Frequency	Max Throughput	Package	Eval Board Order #
DS90CR211MTD	21:3	Transmitter	5	20-40MHz	840Mbps	48TSSOP	–
DS90CR212MTD	21:3	Receiver	5	20-40MHz	840Mbps	48TSSOP	–
DS90CR213MTD	21:3	Transmitter	5	20-66MHz	1.38Gbps	48TSSOP	CLINK5V21BT-66
DS90CR214MTD	21:3	Receiver	5	20-66MHz	1.38Gbps	48TSSOP	CLINK5V21BT-66
DS90CR215MTD	21:3	Transmitter	3.3	20-66MHz	1.38Gbps	48TSSOP	CLINK3V21BT-66
DS90CR216MTD	21:3	Receiver	3.3	20-66MHz	1.38Gbps	48TSSOP	CLINK3V21BT-66
DS90CR281MTD	28:4	Transmitter	5	20-40MHz	1.12Gbps	56TSSOP	–
DS90CR282MTD	28:4	Receiver	5	20-40MHz	1.12Gbps	56TSSOP	–
DS90CR283MTD	28:4	Transmitter	5	20-66MHz	1.84Gbps	56TSSOP	CLINK5V28BT-66
DS90CR284MTD	28:4	Receiver	5	20-66MHz	1.84Gbps	56TSSOP	CLINK5V28BT-66
DS90CR285MTD	28:4	Transmitter	3.3	20-66MHz	1.84Gbps	56TSSOP	CLINK3V28BT-66
DS90CR286MTD	28:4	Receiver	3.3	20-66MHz	1.84Gbps	56TSSOP	CLINK3V28BT-66

LVDS Channel Link Latency

Order Number	Mux/Demux Ratio	Transmitter /Receiver	Power Supply	Clock Frequency	Max Throughput	Latency	TCCD/RCCD Clock Delay (ns) Min	Typ	Max
DS90CR211MTD	21:3	Transmitter	5	20-40MHz	840Mbps	TCCD †	5.0	7.5	10.7
DS90CR212MTD	21:3	Receiver	5	20-40MHz	840Mbps	1 Clock Period + RCCD	7.6	9.0	11.9
DS90CR213MTD	21:3	Transmitter	5	20-66MHz	1.38Gbps	TCCD †	3.5	5.0	8.5
DS90CR214MTD	21:3	Receiver	5	20-66MHz	1.38Gbps	1 Clock Period + RCCD	6.4	8.0	10.7
DS90CR215MTD	21:3	Transmitter	3.3	20-66MHz	1.38Gbps	1 Clock Period + TCCD †	TBD	5.3	TBD
DS90CR216MTD	21:3	Receiver	3.3	20-66MHz	1.38Gbps	2 Clock Periods + RCCD	TBD	6.9	TBD
DS90CR281MTD	28:4	Transmitter	5	20-40MHz	1.12Gbps	TCCD †	5.0	7.5	10.7
DS90CR282MTD	28:4	Receiver	5	20-40MHz	1.12Gbps	1 Clock Period + RCCD	7.6	9.0	11.9
DS90CR283MTD	28:4	Transmitter	5	20-66MHz	1.84Gbps	TCCD †	3.5	5.0	8.5
DS90CR284MTD	28:4	Receiver	5	20-66MHz	1.84Gbps	1 Clock Period + RCCD	6.4	8.0	10.7
DS90CR285MTD	28:4	Transmitter	3.3	20-66MHz	1.84Gbps	1 Clock Period + TCCD †	TBD	5.3	TBD
DS90CR286MTD	28:4	Receiver	3.3	20-66MHz	1.84Gbps	2 Clock Periods + RCCD	TBD	6.9	TBD

† Substitute TCCD = (1/14 clock period + ≈3ns) for a more accurate transmitter latency calculation.
Contact National regarding the latency of future Channel Link devices not listed here.

3.4.0 LVDS FPD-LINK

Use National's FPD Link to convey graphics data from your PC/notebook motherboard to your flat panel displays. The next table summarizes National's FPD Link devices.

LVDS Flat Panel Display Link FPD-Link Solutions

Order Number	Color	Transmitter /Receiver	Power Supply	Max Clock Frequency	Clock Edge Strobe	Package	Eval Board Order #
DS90CF561MTD	18-bit	Transmitter	5	40MHz	Falling	48TSSOP	–
DS90CR561MTD	18-bit	Transmitter	5	40MHz	Rising	48TSSOP	–
DS90CF562MTD	18-bit	Receiver	5	40MHz	Falling	48TSSOP	–
DS90CR562MTD	18-bit	Receiver	5	40MHz	Rising	48TSSOP	–
DS90CF581MTD	24-bit	Transmitter	5	40MHz	Falling	56TSSOP	–
DS90CR581MTD	24-bit	Transmitter	5	40MHz	Rising	56TSSOP	–
DS90CF582MTD	24-bit	Receiver	5	40MHz	Falling	56TSSOP	–
DS90CR582MTD	24-bit	Receiver	5	40MHz	Rising	56TSSOP	–
DS90CF583MTD	24-bit	Transmitter	5	65MHz	Falling	56TSSOP	FLINK5V8BT-65
DS90CR583MTD	24-bit	Transmitter	5	65MHz	Rising	56TSSOP	Use 'CF583 Board
DS90CF563MTD	18-bit	Transmitter	5	65MHz	Falling	48TSSOP	FLINK5V6BT-65
DS90CR563MTD	18-bit	Transmitter	5	65MHz	Rising	48TSSOP	Use 'CF563 Board
DS90CF564MTD	18-bit	Receiver	5	65MHz	Falling	48TSSOP	FLINK5V6BT-65
DS90CR564MTD	18-bit	Receiver	5	65MHz	Rising	48TSSOP	Use 'CF564 Board
DS90CF584MTD	24-bit	Receiver	5	65MHz	Falling	56TSSOP	FLINK5V8BT-65
DS90CR584MTD	24-bit	Receiver	5	65MHz	Rising	56TSSOP	Use 'CF584 Board
DS90C363MTD	18-bit	Transmitter	3.3	65MHz	Programmable	48TSSOP	FLINK3V8BT-65
DS90CF363MTD	18-bit	Transmitter	3.3	65MHz	Falling	48TSSOP	Use 'C363 Board
DS90C383MTD	24-bit	Transmitter	3.3	65MHz	Programmable	56TSSOP	FLINK3V8BT-65
DS90CF383MTD	24-bit	Transmitter	3.3	65MHz	Falling	56TSSOP	Use 'C383 Board
DS90CF384MTD	24-bit	Receiver	3.3	65MHz	Falling	56TSSOP	FLINK3V8BT-65
DS90CF364MTD	18-bit	Receiver	3.3	65MHz	Falling	48TSSOP	FLINK3V6BT-65

Delay/skew units in ns, I_{CC} in mA.

Designing with LVDS

Chapter 4

4.0.0 DESIGNING WITH LVDS

4.1.0 PCB BOARD LAYOUT TIPS

Now that we have explained how LVDS has super speed, and very low power, noise, and cost, many people might assume that switching to LVDS (or any differential technology) will solve all of their noise problems. It will not, but it can help a lot! LVDS has low swing, differential, ≈3.5mA current mode outputs that can help reduce noise/EMI significantly, but these outputs switch (rise and fall) in less than a nanosecond which means many signal paths act as transmission lines. Therefore, knowledge of ultra-high speed board design and differential signal theory is required. Designing high speed differential boards is not difficult or expensive, so familiarize yourself with these techniques *before* you begin your design.

The speed of LVDS means that impedance matching is very important even for short runs. Matching the differential impedance is as important as matching single-ended impedance. Discontinuities in differential impedance **will** create reflections which will degrade the signal and also show up as common mode noise. Common mode noise on the line will not benefit from the cancelling magnetic field effect of differential lines and will be radiated as EMI. You should use controlled differential impedance traces as soon as you can after the signal leaves the IC. Try to keep stubs and uncontrolled impedance runs to <12mm (0.5in). Also, do not make 90° turns since this causes impedance discontinuities, radius or bevel PCB traces.

Minimize skew between conductors within a differential pair. Having one signal of the pair arrive before the other creates a phase difference between voltages along the signal pairs which looks like and radiates as common mode noise.

Use bypass capacitors at each package and make sure each power or ground trace is wide and short (do not use 50Ω dimensions) with multiple vias.

A detailed list of suggestions for designing with LVDS is shown next. The suggestions are inexpensive and easy to implement. By using these suggestions as guidelines, your LVDS-based systems should be quick and easy to develop.

4.1.1 PC Board

a) **Use at least 4 PCB board layers** (top to bottom): LVDS signals, ground, power, TTL signals.

b) **Isolate TTL signals from LVDS signals**, otherwise the TTL may couple onto the LVDS lines. It is best to put TTL and LVDS signals on different layers which are isolated by a power/ground plane(s).

c) Keep drivers and receivers as close to the (LVDS port side) connectors as possible.

d) Bypass each LVDS device and also use distributed bulk capacitance. Surface mount capacitors placed close to power and ground pins work best.

Power Supply: A 10µF 35V tantalum capacitor works well between supply and ground. 4.7µF is common, but choosing a capacitor value which best filters the largest power/ground frequency components (usually 100 to 300MHz) is best. This can be determined by checking the noise spectrum of V_{CC} across bypass capacitors. The voltage rating of tantalum capacitors is critical and must not be less than 5 x V_{CC}. Some electrolytic capacitors also work well.

V_{CC} Pins: Two or three multi-layer ceramic (MLC) surface mount capacitors (0.1µF, 0.01µF, and 0.001µF) in parallel should be used between each V_{CC} pin and ground. The capacitors must be placed as close as possible to the V_{CC} pins. Wide (>4 bits) and PLL-equipped (e.g. Channel Link & FPD Link) LVDS devices should have three capacitors, while other LVDS devices are usually fine with a 0.1µF (possibly also a 0.01µF) capacitor. The bottom line: use good bypassing practices. EMI can be greatly reduced by keeping power and ground planes quiet.

e) **Power and ground should use wide (low impedance) traces.** Do not use 50Ω design rules on power and ground traces.

f) Keep ground PCB return paths short and wide.

g) Cables should employ a ground return wire connecting the grounds of the two systems. See section 5.3.0

h) **Use multiple (at least two) vias to connect to power and ground, traces and planes**. Surface mount capacitors can be soldered directly to these via pads to reduce stubs, though solderability may be impacted.

4.1.2 Traces

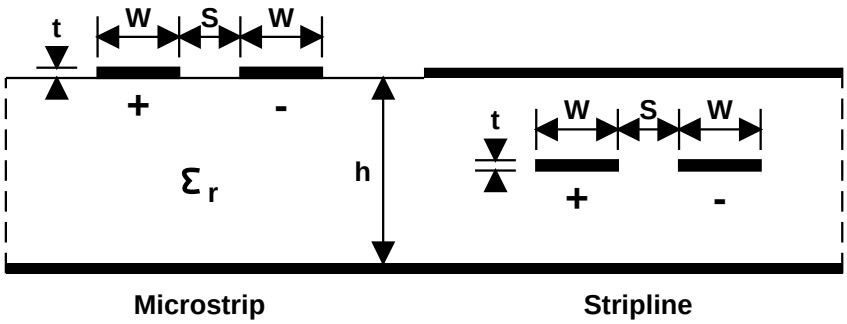
a) Microstrip or stripline both work well.

b) Microstrip offers the advantage that higher differential Z_0 is possible and no extra vias are required.

c) Stripline offers better shielding between signals.

4.1.3 Differential Traces

a) **Use controlled impedance traces which match the differential impedance of your transmission medium (ie. cable) and termination resistor. Run the differential pair trace lines as close together as possible as soon as they leave the IC (stubs should be <10mm long)**. This will help eliminate reflections and ensure noise is coupled as common mode. In fact, we have seen that differential signals which are 1mm apart radiate far less noise than traces 3mm apart since magnetic field cancellation is much better with the closer traces. Plus, noise induced on the differential lines is much more likely to appear as common mode which is rejected by the receiver.



When calculating differential Z_0 (Z_{DIFF}), adjust trace width "W" to alter Z_{DIFF}. Do not adjust "S" which should be the minimum spacing specified by your PCB vendor. You can use National's Transmission Line RapiDesigner slide rule (lit# 633200-001 metric or #633201-001 English units) and app note AN-905, lit# 100905-001) to calculate Z_0 and Z_{DIFF}, or you can use the equations below:

$$Z_{DIFF} \approx 2*Z_0 \left(1 - 0.48e^{-0.96\frac{s}{h}}\right) \text{ Ohms} \quad \text{Microstrip}$$

$$Z_{DIFF} \approx 2*Z_0 \left(1 - 0.347e^{-2.9\frac{s}{h}}\right) \text{ Ohms} \quad \text{Stripline}$$

where

$$Z_0 \approx \frac{60}{\sqrt{0.475\,E_r + 0.67}} \ln\left(\frac{4h}{0.67\,(0.8w + t)}\right) \text{ Ohms} \quad \text{Microstrip}$$

$$Z_0 \approx \frac{60}{\sqrt{E_r}} \ln\left(\frac{4h}{0.67\,\pi\,(0.8w + t)}\right) \text{ Ohms} \quad \text{Stripline}$$

Use consistent (e.g. centimeters only) dimensions for s, h, w, and t.
Cautionary note: The expressions for Z_{DIFF} were derived from empirical data and results may vary.

Common values of dielectric constant (E_r) for various printed circuit board (PCB) materials is given below. Consult your PCB manufacturer for actual numbers. Note that in most LVDS applications, the widely used FR-4 PCB material is acceptable. Teflon is about four times as expensive as FR-4, but can be considered for 100+MHz designs. Also note that E_r will vary within a single board. It is not uncommon for FR-4 PCBs to vary by 10% across one board, affecting skew. This is another good reason to keep differential lines close together.

PCB Material	Dielectric Constant (E_r)	Loss Tangent
Air	1.0	0
PTFE (Teflon)	2.1-2.5	0.0002-0.002
BT Resin	2.9-3.9	0.003-0.012
Polyimide	2.8-3.5	0.004-0.02
Silica (Quartz)	3.8-4.2	0.0006-0.005
Polyimide/Glass	3.8-4.5	0.003-0.01
Epoxy/Glass (FR-4)	4.1-5.3	0.002-0.02

b) Match electrical lengths between traces to reduce skew. Skew between the signals of a pair means a phase difference between signals which destroys the magnetic field cancellation benefits of differential signals and EMI will result! (Note that the velocity of propagation, v = c/E_r where c (the speed of light) = 0.2997mm/ps or 0.0118in/ps).

c) Do not rely solely on the autoroute function for differential traces. Carefully review dimensions to match
differential impedance and provide isolation for the differential lines.

d) Minimize the number of vias and other discontinuities on the line.

e) **Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels instead.**

f) Within a pair of traces, the distance between the two traces should be minimized to maintain common mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable.

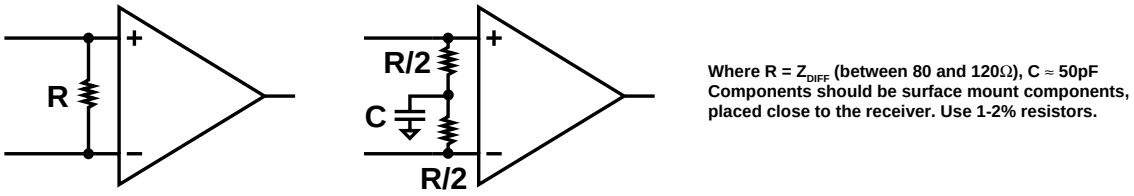
4.1.4 Termination

a) **Use a termination resistor which best matches the differential impedance of your transmission line.** It should be between 90Ω and 130Ω. Remember that the current mode outputs need the termination resistor to generate the differential voltage. LVDS will not work without resistor termination.

b) Typically a single resistor across the pair at the receiver end suffices.

c) Surface mount 1-2% resistors are best. PCB stubs, component leads, and the distance from the termination to the receiver inputs should be minimized. The distance between the termination resistor and the receiver should be <7mm (12mm MAX).

d) Center tap capacitance termination may also be used in conjunction with two ≈50Ω resistors to filter common mode noise at the expense of extra components if desired.



Where R = Z_{DIFF} (between 80 and 120Ω), C ≈ 50pF Components should be surface mount components, placed close to the receiver. Use 1-2% resistors.

Common termination schemes.

4.1.5 Unused Pins

a) **Leave unused LVDS receiver inputs open (floating).** Their internal fail-safe feature will lock the outputs high. These unused receiver inputs should not be connected to noise sources like cables or long PCB traces — float them near the pin.

b) Leave all unused LVDS and TTL outputs open (floating) to conserve power.

c) Tie unused TTL transmitter/driver inputs and control/enable signals to power or ground.

4.1.6 Probing LVDS Transmission Lines

a) **Always use a high impedance (>100kΩ), low capacitance (<0.5pF) scope probes with a wide bandwidth (>3GHz) scope.** Improper probing *will* give deceiving results.

4.1.7 Loading LVDS I/O

a) Avoid placing any devices which heavily load the low, ≈3.5mA LVDS output drive. If additional ESD protection devices are desired, use components which do not add a significant load to the LVDS output. Some of the connectors with integrated polymer ESD protection are a good option.

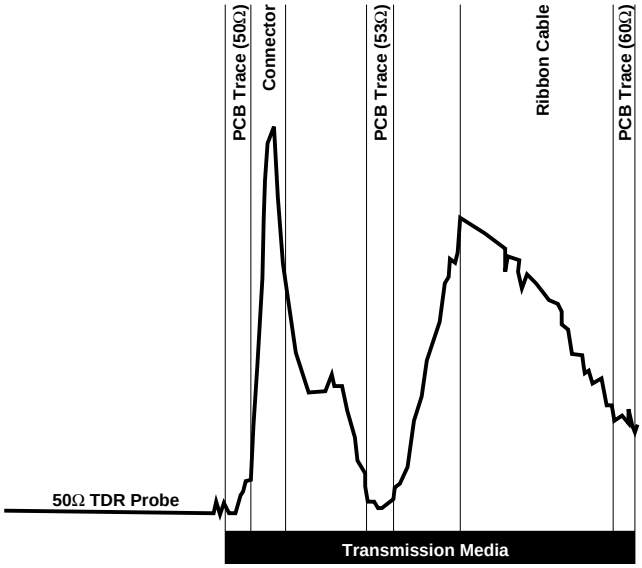
b) Try not to disturb the differential balance. Treat both members of a pair equally.

4.2.0 RESULTS OF GOOD VS. BAD DESIGN PRACTICES

4.2.1 Impedance Mismatches

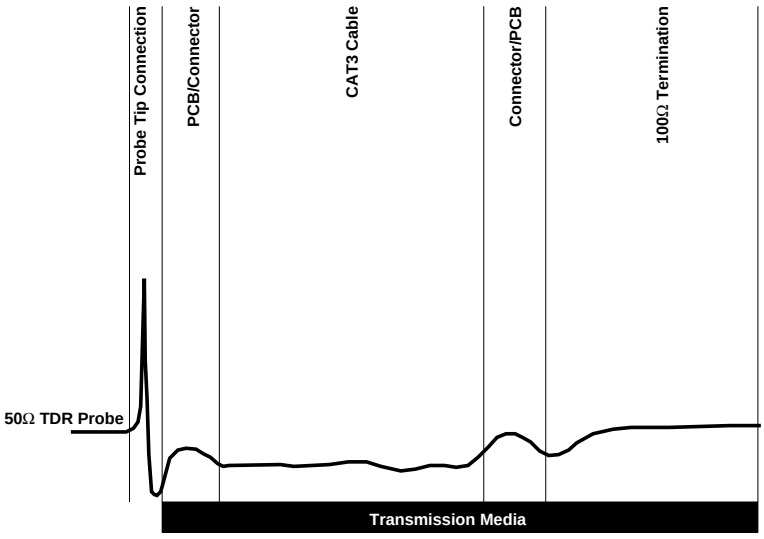
It is very common for designers to automatically use any off-the-shelf cables and connectors and 50Ω autorouting when doing new designs. While this may work for some LVDS designs, it can lead to noise problems. Remember that LVDS is differential and does have low swing, current mode outputs to reduce noise, but that its transition times are quite fast. This means impedance matching (especially differential impedance matching) is very important. Those off-the-shelf connectors and that cheap blue ribbon cable

are not meant for high speed signals (especially differential signals) and do not have controlled impedance. The figure below shows a time-domain reflectometer (TDR) impedance trace of such a system. As one can plainly see, impedance are neither matched nor controlled. Beware, this example is not worst case — it is a typical example reflecting common TTL design practices. The reflections caused by impedance mismatching will generate a lot of noise and EMI.



TDR plot of transmission media with mismatched impedance.

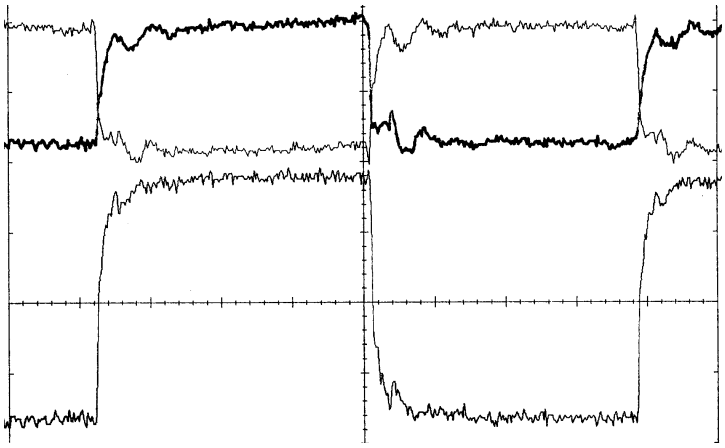
Below is a much improved design which follows most of the high speed differential design practices listed in Section 4.1. The TDR differential impedance plot is much flatter and noise is **dramatically** reduced.



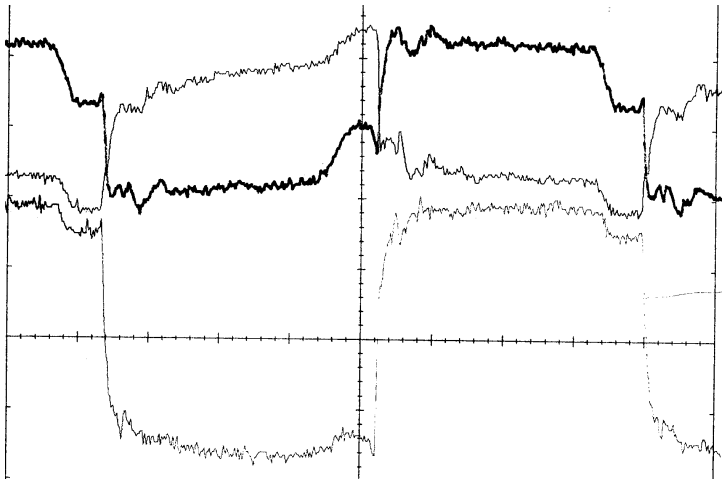
Minimize impedance variations for best performance.

4.2.2 Crosstalk Between TTL and LVDS Signals

The next two figures show the effects of TTL coupling onto LVDS lines. The first figure shows the LVDS waveforms before coupling, while the second shows the effects of a 25MHz, 0V to 3V TTL signal upon the LVDS signals running adjacent for 4 inches. The result is an LVDS waveform modulated by the TTL signal. Note that the LVDS pair is not affected exactly equally — the signal which runs closest to the TTL trace is affected more than the other. This difference will not be rejected by the receiver as common mode noise and though it will not falsely trigger the receiver, it does degrade the signal quality of the LVDS signal reducing noise margin. The common mode noise will be rejected by the receiver, but can radiate as EMI.



LVDS signals before crosstalk.



LVDS signals affected by TTL crosstalk.

In summary, place TTL signals at least 12mm away from LVDS signals or place a power or ground plane between them.

4.3.0 LOWERING ELECTROMAGNETIC INTERFERENCE (EMI)

4.3.1 LVDS and Lower EMI

High speed data transmission usually means fast edge rates and high EMI. LVDS, however, has many positive attributes that help lower EMI:

1) The low output voltage swing (≈350mV)

2) Relatively slow edge rates, dV/dt ≈ 0.350V/0.5ns = 0.7 V/ns

3) Differential (odd mode operation) so magnetic fields tend to cancel

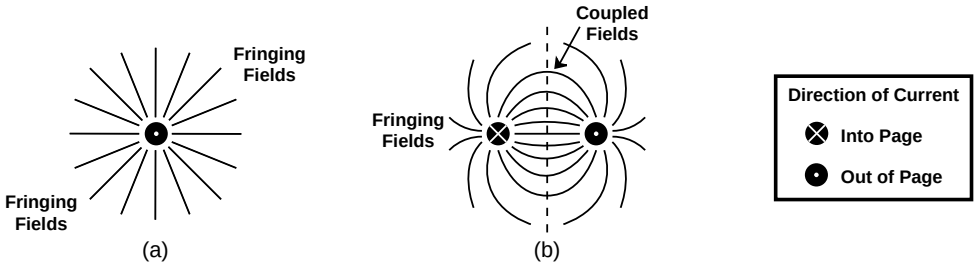
4) "Soft" output corner transitions

5) Minimum I_{CC} spikes due to low current mode operation

To realize these advantages, however, designers must take care to ensure the close proximity of the pair conductors and to avoid creating impedance imbalances within a pair. The following sections describe these EMI-friendly design practices.

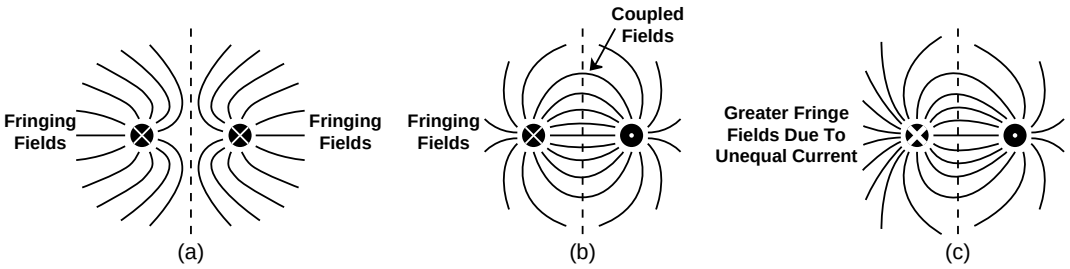
4.3.2 Electromagnetic Radiation of Differential Signals

Today's increasing data rates and tougher electromagnetic compatibility (EMC) standards are making electromagnetic radiation an increasing concern. System designers are usually most concerned with far field electromagnetic radiation, propagated through transverse electromagnetic (TEM) waves which can escape through shielding causing a system to fail EMC tests. Fields around a conductor are proportional to voltage or current, which are small in the case of LVDS. The fields are distorted by and interact with their environment, which is why EMI is so hard to predict. The fields can be distorted to advantage, however, and such is the case with tightly coupled differential lines ("+" and "–" signals in close proximity with one another). In single-ended lines like CMOS/TTL shown below, almost all the electric field lines are free to radiate away from the conductor. These fields may be intercepted by other objects, but some can travel as TEM waves which may escape the system causing EMC problems.



Electromagnetic field cancellation in differential signals (b) through coupling versus a single-ended signal (a).

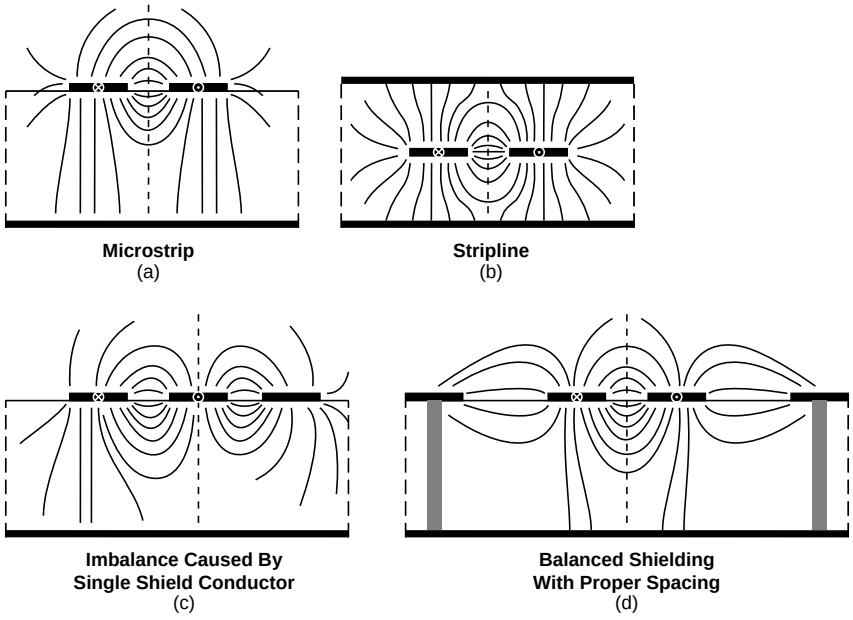
Balanced differential lines, however, have equal but opposite ("odd" mode) signals. This means that the concentric magnetic fields lines tend to cancel and the electric fields (shown above) tend to couple. These coupled electric fields are "tied up" and cannot escape to propagate as TEM waves beyond the immediate vicinity of the conductors. Only the stray fringing fields are allowed to escape to the far field. Therefore, for coupled differential signals much less field energy is available to propagate as TEM waves versus single-ended lines. The closer the "+" and "–" signals, the tighter or better the coupling.



Even or common mode signals (a), ideal equal and opposite odd mode signals (b), and unbalanced signals (c) on differential lines.

Clearly, the voltages and currents of the two ("+" and "–") conductors are not always equal and opposite. For LVDS, the DC currents should never flow in the same direction as in (a) above, but factors can cause an imbalance in currents (c) versus the ideal case in (b). When this imbalance happens, an excess of field fringing occurs since the field strength of the two conductors is unequal. The extra fringe fields can escape as TEM waves and lead to more EMI.

Similar effects can be seen in microstrip and stripline PCB traces shown below. The ideal cases for microstrip and stripline are represented by (a) and (b). Here we see that the microstrip ground plane helps couple additional field lines from below, tying up more field lines and reducing EMI. Stripline almost completely shields the conductors and therefore can significantly decrease EMI, but has the penalty of slower propagation velocity (about 40% slower than microstrip), more PCB layers, additional vias, and difficulty in achieving 100Ω Z_{0DIFF}. More shielding can be achieved using microstrip without significantly impacting propagation velocity using shield traces as in (d), but be careful to add the shield trace (preferably ground) on both sides of the pair (d). Running the shield trace — or any trace — on one side (c) creates an imbalance which can increase EMI. Ground trace shields should have frequent vias to the underlying ground plane at regular (<1/4 wavelength) intervals, and should be placed at least 2s from the pair.

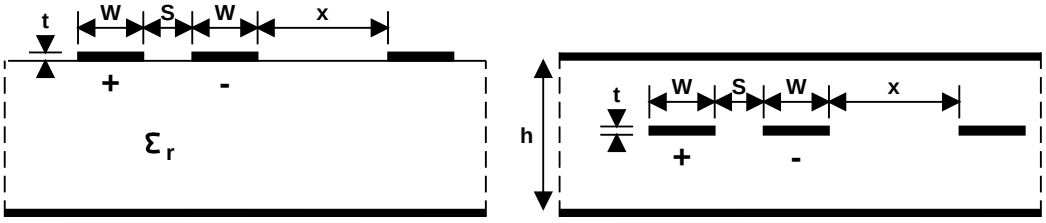


Ideal differential signals on microstrip a) and stripline (b), negative effects of unbalanced shielding (c), and positive effects of balanced shielding (d).

4.3.3 Design Practices for Low EMI

As discussed in the preceding paragraphs, the two most important factors to consider when designing differential signals for low EMI are close coupling between the conductors of each pair and minimizing the imbalances between the conductors of each pair. Let us discuss close coupling first.

In order for sufficient coupling to occur, the space between the conductors of a pair should be kept to a minimum as shown below. (Note that matched transmission impedance must also be maintained). Stripline power and ground planes/traces should not be closer than the distance between conductors to preserve closer coupling between the conductors versus the power and ground planes. A good rule is to keep S < W, S < h, and x greater or equal to the larger of 2S or 2W. The best practice is to use the closest spacing, "S," allowed by your PCB vendor and then adjust trace widths, "W," to control differential impedance.

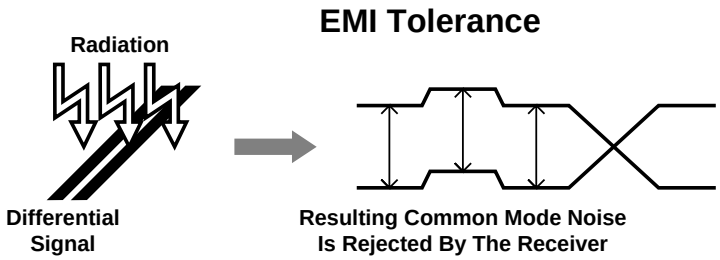


Microstrip **Stripline**

For good coupling, make S < 2W, S < h, and x ≥ 2W & 2S.

For sufficient coupling (cancelling) of electromagnetic fields, "+" and "–" signal distance must be minimized.

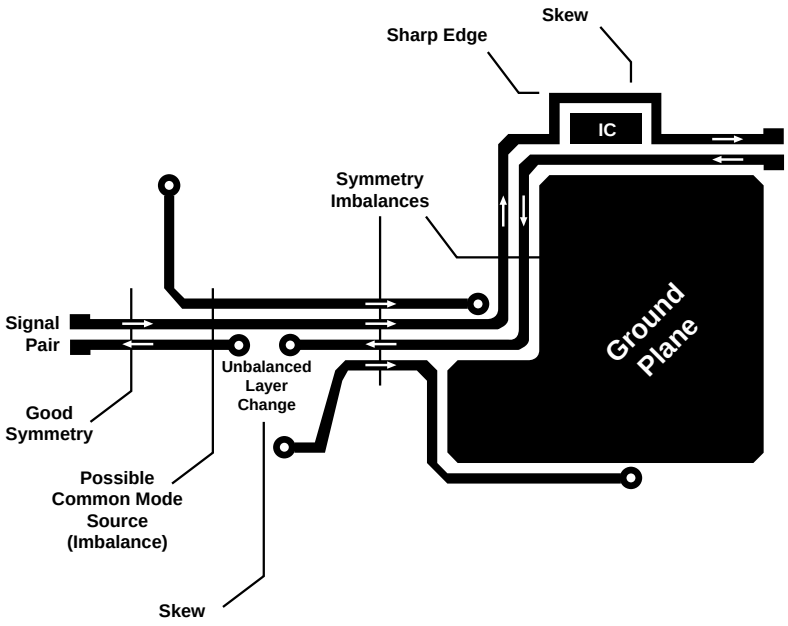
Close coupling between conductors of a pair not only reduces EMI, but it helps to ensure noise coupled onto the conductors will do so equally as common mode noise which will then be rejected by the receiver. Since the differential pair is a current loop, minimizing conductor spacing also reduces the antenna loop.



Close coupling not only reduces EMI, but improves EMI tolerance too.

Imbalance minimization is the other important factor in reducing EMI. Although fields result from the complex interaction between objects of a system and are difficult to predict (especially in the dynamic case), certain generalizations can be made. The impedance of your signal traces should be well-controlled. If the impedance of one trace changes versus another, the voltage and fields of one signal will be different from its partner. This will tend to create more fringing fields and therefore more EMI as we have seen.

The basic rule to follow is: if any discontinuity must be introduced in proximity to differential lines, it should introduced equally to both members of the pair. Examples of discontinuities include: components, vias, power and ground planes, PCB traces, etc. Remember, the key word is **balance**.



This PCB layout contains many sources of differential signal imbalance that will tend to increase electromagnetic radiation.

Unfortunately unless you have an elaborate EMI lab, fields resulting from imbalances cannot easily be measured. Waveforms, however, are easy to measure. Since fields are proportional to voltage/current amplitude at any given point in time, any factors affecting the time (delay, velocity, etc.) and/or amplitude (attenuation, etc.) properties of the signals can increase EMI and can be seen on a scope. The next figure illustrates how waveforms — easily seen on a scope — can help predict far field EMI. First, the beneficial field cancelling effects of ideal differential signals (b) versus single-ended signals (a) are compared.

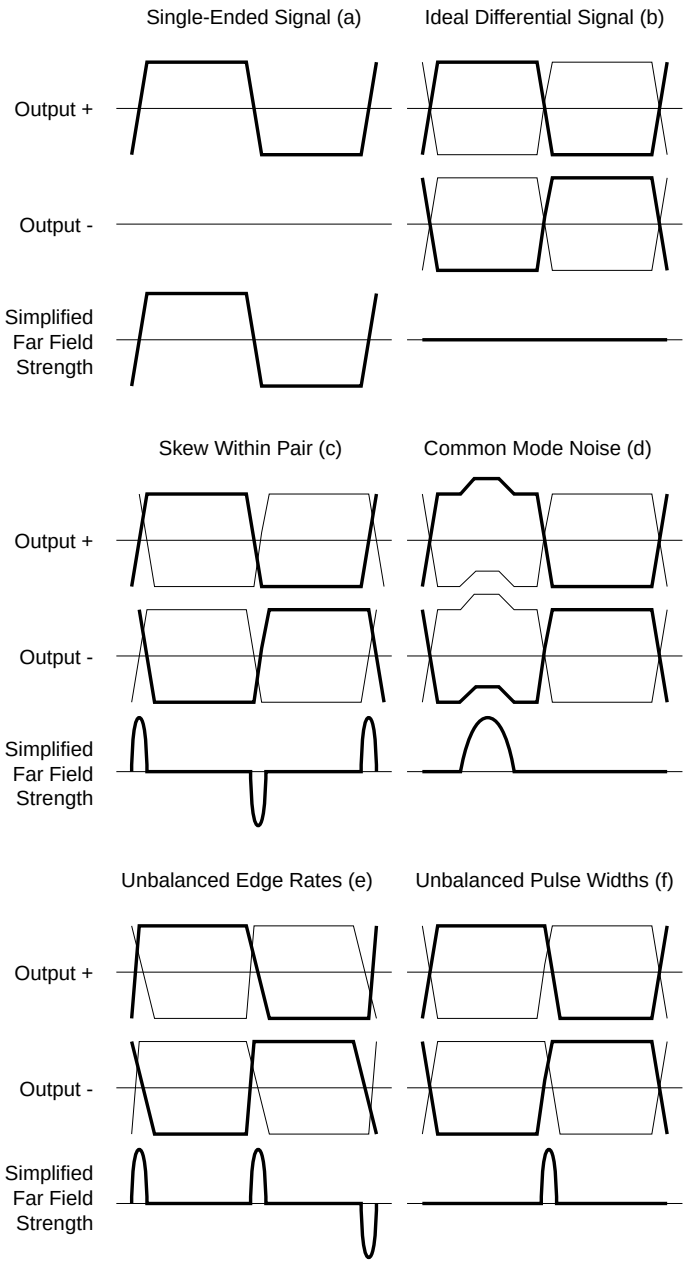
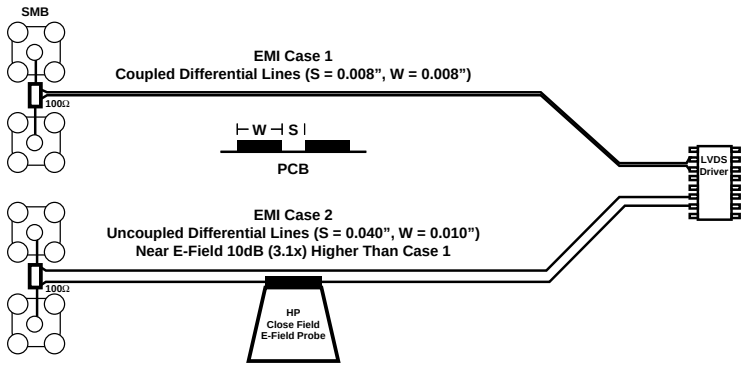


Diagram showing simplified far field radiation under various situations.

A real differential signal, however, is non-ideal and contains skew, unbalanced pulse widths and edge rates, common mode noise, unbalanced attenuation, etc. These affect the relative amplitudes of the fields at any given moment, reducing the cancelling effects of the differential signals, and potentially increasing EMI. Thus, the waveforms of one conductor of a pair should balance or mirror the other to minimize EMI.

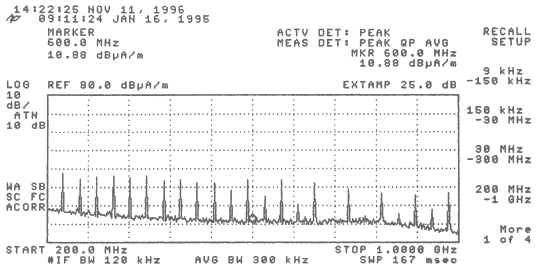
4.3.4 EMI Test Results

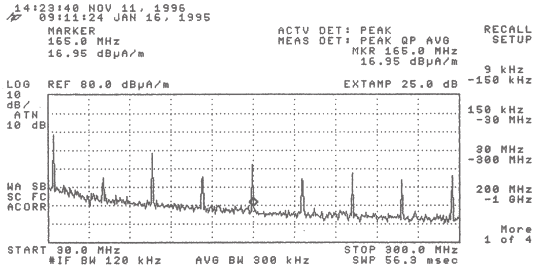
The PCB setup shown below was used to examine the effects on EMI of closely coupled differential signals versus uncoupled signals. The setup compares two sets of LVDS signals: one set in which pair spacing is less than trace width (S<W) and another set in which S>>W so that the pair members are no longer closely coupled (though the differential impedance of the transmission line is still 100Ω).



EMI Test Setup

Near (close) field electric field measurements were made for both cases while using a 32.5MHz 50% duty cycle clock as the source. The two plots below show the E-field strength results for case 2, the uncoupled case. The first plot shows the E-field strength over 200MHz to 1GHz. The second plot looks more closely at the frequencies between 30MHz and 300MHz. The electric field noise shows up as "spikes" which occur at harmonics of the input frequency.

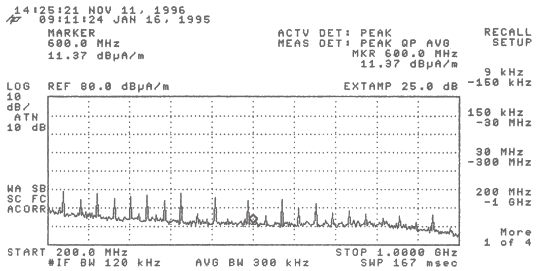


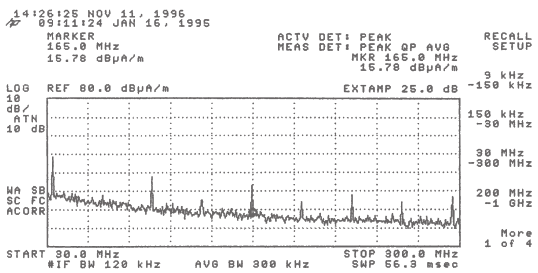


Near E-Field Strength for Uncoupled Signals

(Case 2): 200MHz-1GHz *(Case 2): 30MHz-300MHz*

The next two plots show the E-field strength for case 1 in which the differential pair is closely coupled. Notice that the harmonics are significantly reduced.





Near E-Field Strength for Closely Coupled Signals

(Case 1): 200MHz-1GHz *(Case 1): 30MHz-300MHz*

In the far field, the EMI of the closely coupled pair should radiate much less due to the coupling of the electric fields. Even in the near field, however, the closely coupled pair generated much weaker electric fields. The closely coupled pair showed about 10dB (>3 times) lower electric field strength than the uncoupled pair.

This test illustrates two things:

1) Use of differential signals versus single-ended signals can be used effectively to reduce emissions.

2) The EMI advantages of differential signs will be lost or greatly diminished unless the signals are closely coupled.

This test used uncoupled LVDS signals to represent single-ended signals. Most single-ended signals such as TTL or GTL, have a much greater swing and involve much greater currents, so their EMI is expected to be even greater than is seen here.

4.3.5 Ground Return Paths

A conductor that carries current requires an opposite mirror current to return through some part of the system. This return current path will be the path of least impedance.

Since LVDS is differential, differential current that flows in one conductor of a pair will flow back through the other conductor, completing the current loop. This is ideal, because the current return antenna loop area is minimized since the traces of a pair are closely spaced. Real signals, however, will have some common mode noise current which must return also. This common mode current will be capacitively coupled to ground and return to the driver through the path of least impedance. Therefore, a short ground current return path is needed between the driver and receiver in differential systems as well as single-ended (though to a lesser extent).

On PCBs, the best current return path is a uniform, unbroken ground plane beneath the LVDS signals. The ground plane will allow the common mode (even mode) current to return directly under the LVDS signals. This closely coupled path is the path of least impedance and means that the current loop area is minimized.

Similarly, in cable ground return wire or wires should be used between driver and receiver. This allows the return path to be in close proximity to the signal pairs reducing the current loop area (see Chapter 5).

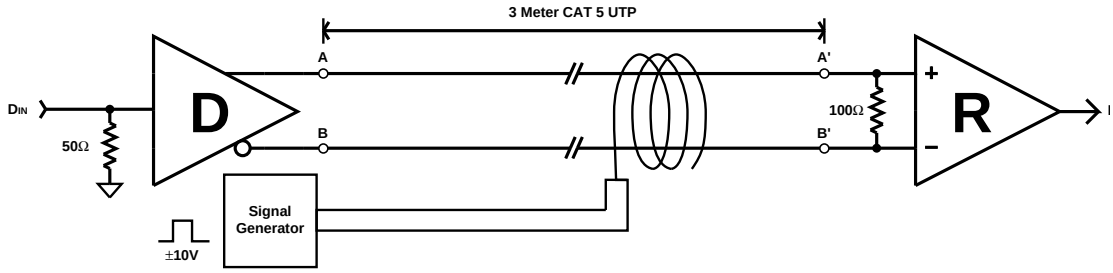
4.3.6 Cable Shielding

Shielding is an effective way to reduce EMI. Shielding should be connected directly to both driver enclosure and receiver enclosure when possible. Many shields are not designed to handle significant ground return currents, so it may be necessary to construct a filter network which isolates the shield from ground at one end (see Chapter 5).

4.3.7 Conclusion

To take advantage of the inherent low EMI properties of LVDS, designers should ensure the conductors of each pair are (1) closely coupled and (2), well-balanced. Impedance, both single-ended and differential, should be controlled.

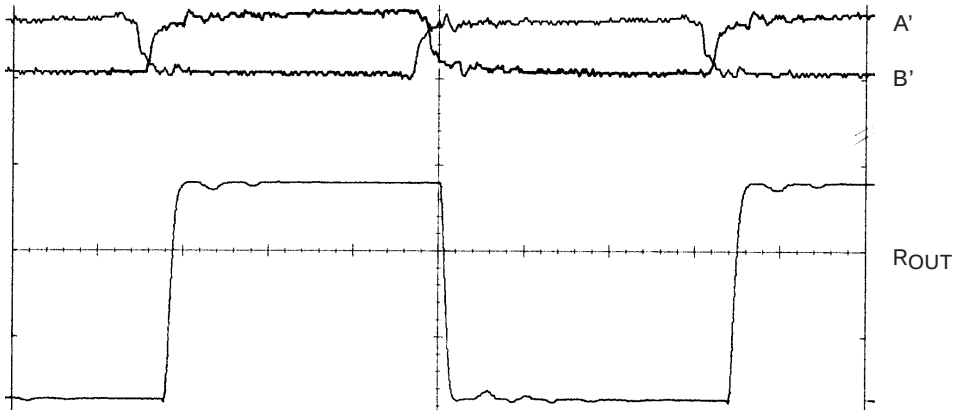
4.4.0 COMMON MODE NOISE REJECTION



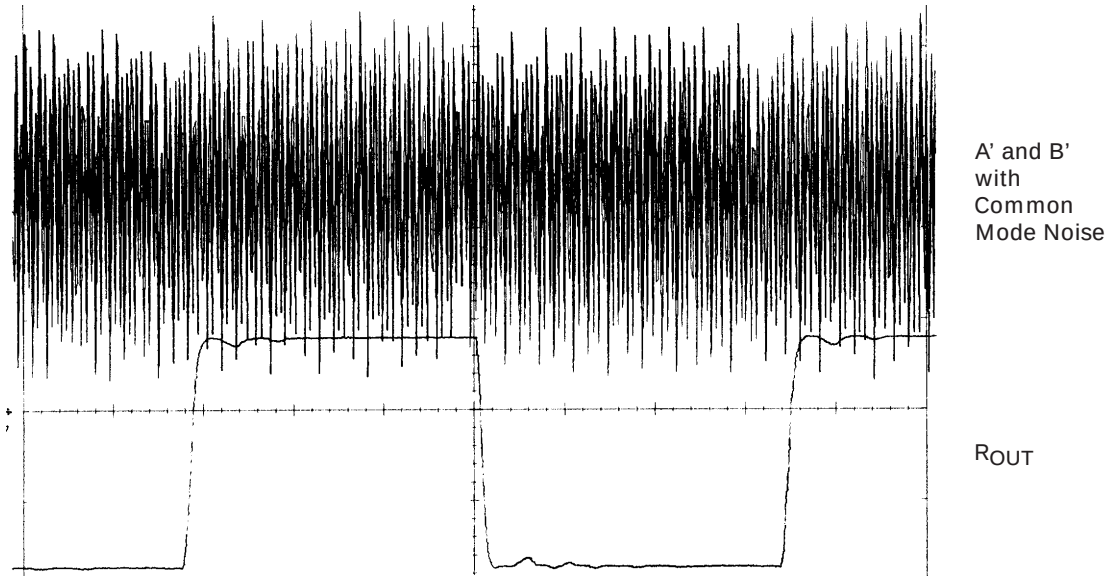
Common mode noise rejection test setup.

Test Setup:
Driver: DS90C031 (one channel)
Receiver: DS90C032 (one channel)
V_{CC} = 5V
T = 25°C

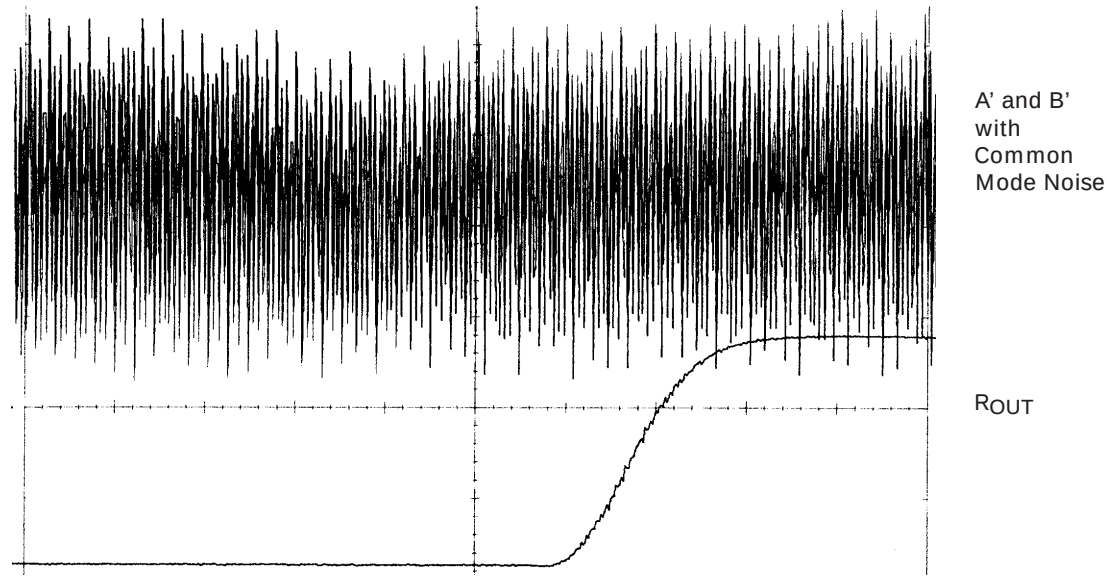
This test demonstrates the common mode noise rejection ability of National's LVDS receivers. Some have expressed concern over the noise immunity of LVDS because of its low voltage swing (≈±350mV swing with <±100mV thresholds). Provided that the differential signals run close together through controlled impedance media, however, most of the noise on LVDS lines will be common mode. In other words, EMI, crosstalk, power/ground shifts, etc. will appear equally on each pair and this common mode noise will be rejected by the receiver. The plots below show common mode noise rejection with VCM noise up to –0.5V to +3.25V peak-to-peak.



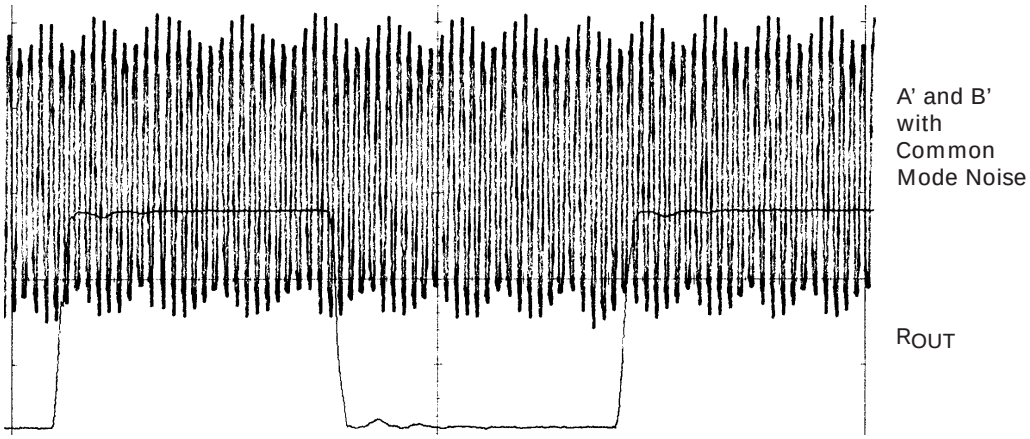
Reference waveform showing LVDS signal and receiver output.



Coupled common mode noise of 0.5V to 1.75V peak-to-peak and resulting clean receiver output.

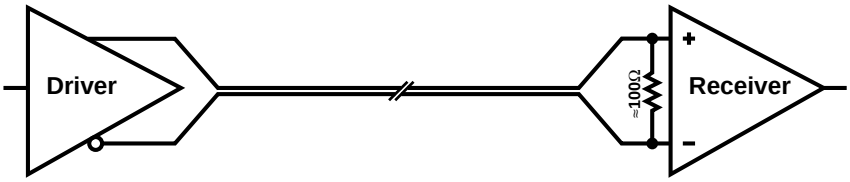


Expanded view of coupled common mode noise waveform and clean receiver output.



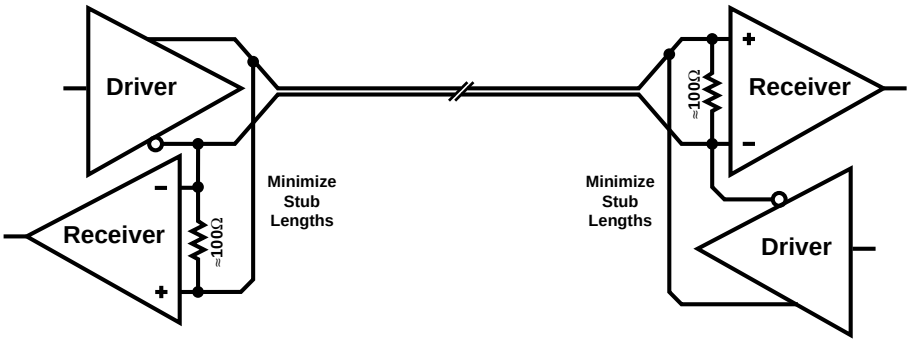
Clean receiver output despite –0.5V to +3.25V peak-to-peak common mode noise.

4.5.0 LVDS CONFIGURATIONS

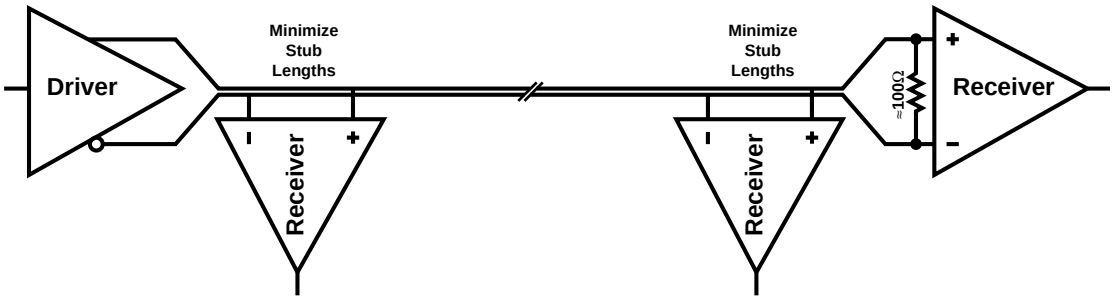


Point-to-point configuration.

Although LVDS drivers and receivers are typically used in a point-to-point arrangement (above), other topologies are possible. The configuration shown below allows bi-directional communication over a single twisted pair. Data can flow in only one direction at a time. The requirement for two terminating resistors reduces the signal (and thus the differential noise margin), so this configuration should be considered only where noise is low and transmission distance is short (≤10m). Typical LVDS I/O capacitances are 5-7 pF for receiver inputs and 3.5-4pF for driver outputs.



Bi-directional half-duplex configuration.



Multidrop configuration.

Since LVDS receivers have high impedance inputs, a multidrop configuration can also be used if transmission distance is short and stub lengths are less than 12mm (<7mm is recommended). Use receivers with power-off high impedance if the network needs to remain active when one or more nodes are powered down.

4.6.0 FAIL-SAFE FEATURE

4.6.1 Most Applications

To help ensure reliability, LVDS receivers have internal fail-safe circuitry that forces the output to be in a known logic state (HIGH) under certain fault conditions. These conditions include open, shorted, and terminated receiver inputs. Here is a summary of LVDS fail-safe conditions:

1) Open Input Pins
   Unused receiver inputs should be left OPEN. Do not tie unused receiver inputs to ground or other voltages. The internal failsafe bias resistors will pull the "+" input high, and the "–" input low, thus guaranteeing a high, stable output state.

2a) Terminated Input Pins
   If the driver is in a TRI-STATE® condition, in a power-off condition, or is disconnected (cable unplugged), the receiver output will be in a high state, even with the termination resistor across the input pins.

2b) Terminated Input Pins — Noisy Environments
   See section 4.6.2 if fail-safe must be guaranteed in noisy environments when the cable is disconnected from the driver end or the driver is in TRI-STATE®.

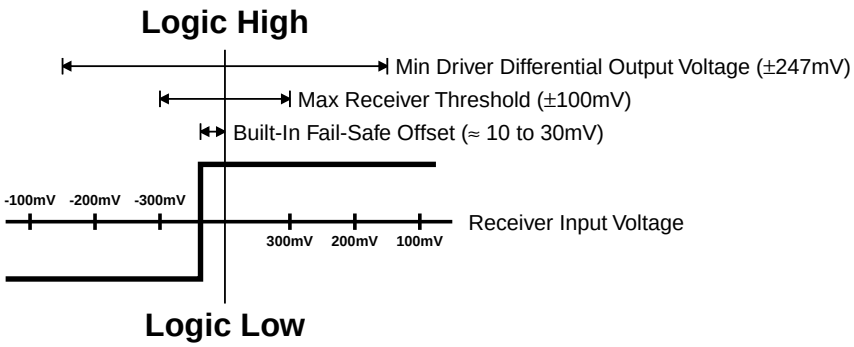
3) Shorted Inputs
   The receiver output will remain in a high state when the inputs are shorted.

4.6.2 Boosting Fail-Safe In Noisy Environments

The internal fail-safe circuitry is designed to source/sink a small amount of current, providing fail-safe protection for floating receiver inputs, shorted receiver inputs, and terminated receiver inputs. It is not designed to provide fail-safe in noisy environments when the cable is disconnected from the driver end or the driver is TRI-STATE. When this happens, the cable becomes a floating antenna which can pick up noise. If the cable picks up more differential noise than the internal fail-safe circuitry can overcome, the receiver may switch or oscillate. If this condition can happen in your application, it is recommended that you choose a balanced and/or shielded cable which will reduce the amount of differential noise on the cable. In addition, you may wish to add external fail-safe resistors to create a larger noise margin. However, adding more fail-safe current will tend to unbalance the symmetrical LVDS output drive (loop) current and degrade signal quality somewhat. Therefore a compromise should be the ultimate goal.

4.6.3 Choosing External Fail-Safe Resistors

Typical Differential Input Voltage (V_{ID}) vs. Receiver Logic State



External fail-safe can be added, but must be small enough not to significantly affect driver current.

The chart above shows that National's present LVDS devices typically have an internal fail-safe voltage of about 10 to 30mV. If the receiver will not always be driven by the driver in your application and the cable is expected to pick up more than 10mV of differential (not common mode) noise you may need to add additional fail-safe resistors. The resistors are chosen by first measuring the amount of differential mode noise you will need to overcome, V_{FSB}, by biasing the termination resistor (≈100Ω) to generate this voltage. Note that you do not need to provide a bias, V_{FSB}, which is greater than the receiver threshold (100mV). You only need enough to overcome the differential noise, since the internal fail-safe circuitry will always guarantee a positive offset. In fact, making V_{FSB} too large will contend with the driver output causing the driven signal to become imbalanced and reduce signal quality.

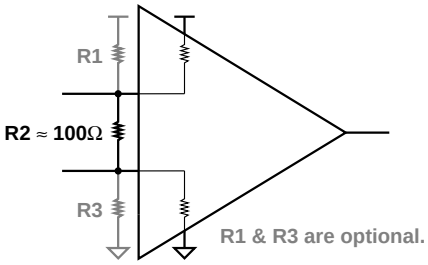


Diagram showing simplified internal fail-safe circuitry and optional external "helper" fail-safe resistors.

For best results, follow these procedures when choosing external fail-safe resistors:

1) First ask the question "Do I need external fail-safe?" If your LVDS driver is always active, you will not need external fail-safe. If the cable is never disconnected from the driver end while the system is active and/or your cable will not pick up much differential mode noise you may not need to boost fail-safe.

2) Measure the amount of **differential (odd) mode** noise at the receiver end of the cable in worst case conditions. If you have a lot of noise, **use a balanced cable** like twisted pair which tends to pick up mostly common mode noise , not differential mode noise. Do not use simple ribbon or coax cables which can pick up differential mode noise.

   Use a **shielded cable** if possible. Using a balanced and/or shielded cable is best way to prevent instead of fix the noise issue!

3) Once you have chosen the appropriate cable, measure the amount of differential voltage at the receiver under worst case conditions. Set this equal to V_{FSB} in the equation below and solve for the external fail-safe resistors R1 and R3.

$$V_{FSB} = \frac{R2}{R1 + R2 + R3} V_{CC}$$

$$I_{BIAS} = \frac{V_{CC}}{R1 + R2 + R3} << I_{LOOP} \quad (\text{Use } I_{BIAS} \leq 0.1 * I_{LOOP})$$

$$V_{CM} = \frac{R3 + R2/2}{R1 + R2 + R3} V_{CC} = 1.2V \Rightarrow R1 \approx R3 \left(\frac{V_{CC}}{1.2V} - 1 \right)$$

$$R_{TEQ} = \frac{R2\,(R1 + R3)}{R1 + R2 + R3} = \text{match transmission line } Z_{0DIFF}$$

4) You now have an equation relating R1 to R3. Choose R1 and R2 so that: (1) they approximately satisfy the third equation for V_{CM} = 1.2V, and (2) they are large enough that they do not create a bias which will contend with the driver current (I_{BIAS} << I_{LOOP}, equation two). In general, R1 and R2 should be greater than 20kΩ for V_{CC} = 5V and greater than 12kΩ for V_{CC} = 3.3V. **Remember that you want just enough I_{BIAS} to overcome the differential noise, but not enough to significantly affect signal quality.**

5) The external fail-safe resistors may change your equivalent termination resistance, R_{TEQ}. Fine tune the value of R2 to match R_{TEQ} to within about 10% of your differential transmission line impedance.

4.7.0 POWER OFF HIGH IMPEDANCE

Power off high impedance is a useful feature:

1) For receivers which might be powered down while the driver is active. Note that since LVDS drivers only source about 3.5mA of current, NOT having power off high impedance may be acceptable.

2) For receivers in multi-drop mode when the network must remain operational if one or more receivers are powered down.

3) For drivers, receivers, and transceivers in multi-point or bidirectional applications when the network must remain operational if one or more receivers are powered down or live insertion capability is desired.

LVDS devices will behave differently during power down. Here is a summary of power off conditions and the results to various devices:

a) Driver power OFF, receiver power ON:

- LVDS receivers have fail-safe to avoid oscillation.
- LVDS quad, dual, and single receivers outputs will be locked to logic high.
- LVDS Channel Link and FPD-Link device outputs will remain in last known state until clocked at which point the outputs will lock high.
- Some driver outputs will power off to high impedance (check datasheet).

b) Driver power ON, receiver power OFF:

- 5V receivers will sink driver current, but since this current is small, it will not damage the driver (transmitter) or receiver.
- 3V receiver inputs will power off to high impedance.

Cables and Connectors

Chapter 5

5.0.0 MEDIA (CABLE AND CONNECTOR) SELECTION

5.0.1 General Comments

When choosing cables and connectors for LVDS it is important to remember:

1) Use controlled impedance media. The cables and connectors you use should have a matched differential impedance of about 100Ω. They should not introduce major impedance discontinuities.

2) Balanced cables (e.g. twisted pair) are usually better than unbalanced cables (ribbon cable, simple coax) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation as common mode (not differential mode) noise which is rejected by the receiver.

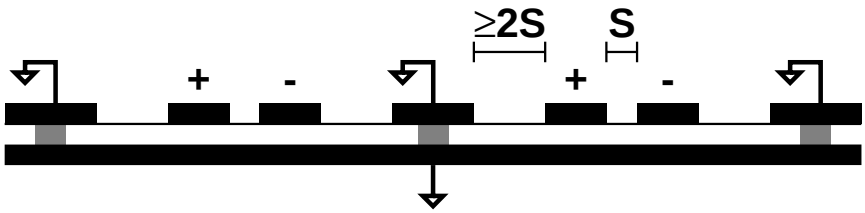
3) For cable distances <0.5m, most cables can be made to work effectively. For distances 0.5m ≤ d ≤ 10m, CAT 3 (category 3) twisted pair cable works well and is readily available and relatively inexpensive. For distances >10m, and high data rates CAT 5 twisted pair is recommended.

5.2.0 CABLING SUGGESTIONS

As described above, try to use balanced cables (twisted pair, twinax, or flex circuit with closely coupled differential traces). Whatever cable you do choose, following the suggestions below will help you achieve optimal results.

5.2.1 Flex Circuit

Flex circuit is a good choice for short runs, but it is difficult to shield.



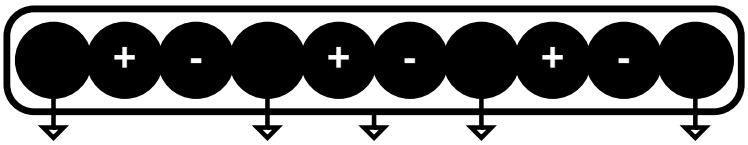
a) Closely couple the members of differential pairs (S<W). Do not run signal pairs near the edges of the cable.

b) Use a ground plane.

c) Use ground shield traces between the pairs if there is room. Connect these ground traces to the ground plane through vias at frequent intervals.

5.2.2 Ribbon Cable

Ribbon cable is cheap and is easy to use and shield. Ribbon cable is not well-suited for high speed differential signaling (good coupling is difficult to achieve), but it is OK for short runs.

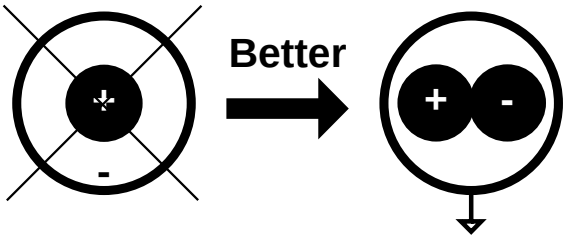


a) If ribbon cable must be used, separate the pairs with ground wires. Do not run signal pairs at the edges of the ribbon cable.

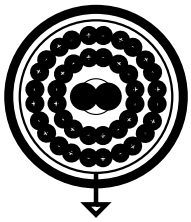
b) Use shielded cable if possible.

5.2.3 Twinax and Coax

Coax is not balanced, so twinax is much better for LVDS.



5.2.4 Twisted Pair

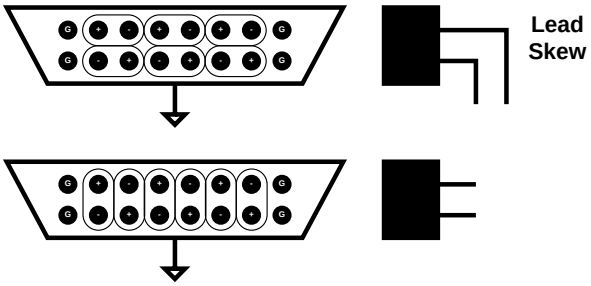


a) Twisted pair is a good choice for LVDS. Category 3 (CAT3) cable is good for runs up to about 10m, while CAT5 is better for longer runs.

b) For lowest skew, group skew-dependent pairs together (towards the center or towards the outside of the cable).

c) Ground and/or terminate unused conductors.

5.2.5 Connectors



a) Choose low skew, impedance matching connectors if possible.

b) Group members of each pair together. **Be sure that the pin assignment you choose on the connector matches the orientation of the pairs. In other words, a pair may be pins 1 and 26 not pins 1 and 2.**

c) Some connectors have different length leads for different pins. Group pairs on same length leads. Consult the connector manufacturer for the orientation of pins which yield the lowest skew and crosstalk for your particular connector.

d) Place ground pins between pairs where possible and convenient.

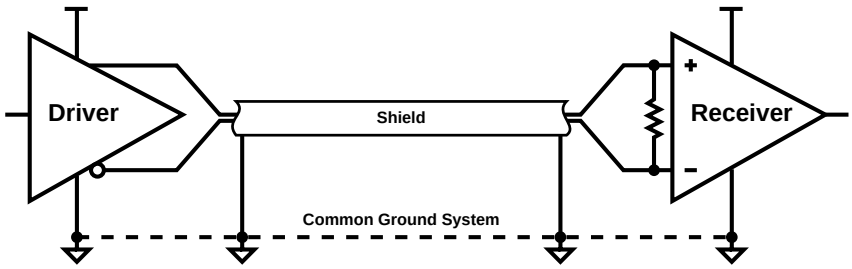
e) Ground end pins. Do not use end pins for high speed signals.

f) Ground and/or terminate unused pins.

5.3.0 CABLE GROUND AND SHIELD CONNECTIONS

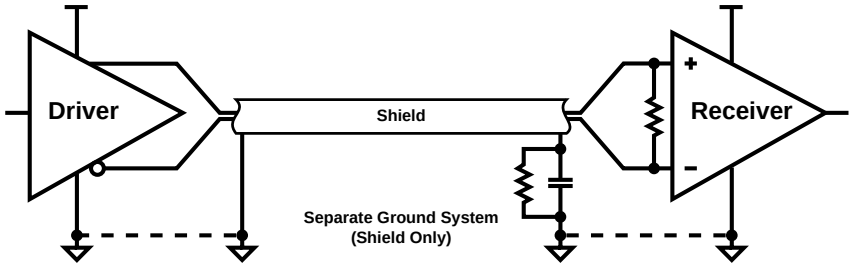
In many systems, cable shielding is required for EMC compliance. Although LVDS provides low EMI benefits when used properly, shielding is still usually a good idea. Together, cable shielding and ground return wires help reduce EMI. The shielding contains the EMI and the ground return wire (the shield in some cables) provides a small loop area AC return path for common mode currents. **Note: it is beyond the scope of this book to effectively deal with cabling systems in detail. Please consult other texts on this subject and be sure to follow applicable safety and legal requirements for cabling, shielding and grounding.**

5.3.1 Common Ground Systems

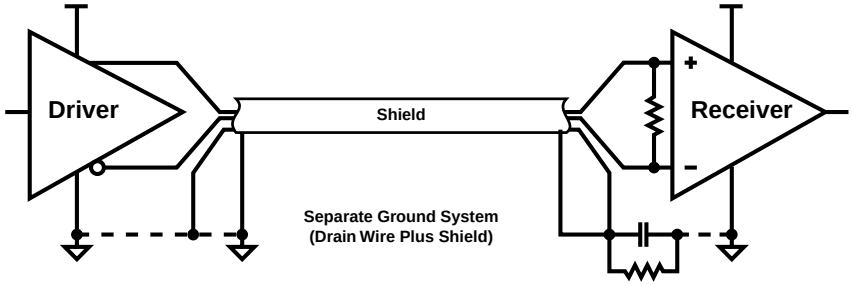


In applications where the grounding system will be common to both the receiver and the driver, the cable shield is connected at both ends (DC connection) to the common ground. Avoid “pig-tail” ground wiring from the cable. In the case where connectors are involved that penetrate the system’s enclosure, the cable shield must have a circumferential contact to the connector’s conductive backshell.

5.3.2 Separate Ground Systems



Where AC and/or DC voltage potentials exist between the driver and receiver sub-systems or where these do not share a common ground system, the cable shield should be connected to the receiver's ground system via a capacitor of suitable value and voltage rating to handle the average DC and peak AC voltages that may be present. A "bleeder resistor" should be connected across the capacitor. The value of this resistor (and capacitor) may be governed by safety requirements (UL, CSA, VDE, BS, or other) or other statutory requirements. Care should be taken when selecting the resistor value so as not to allow potentially lethal voltages to be developed across it.



When the cable has an integral drain wire and a woven braid shield, both are connected together at the driver and receiver ends and treated as a common shield conductor. For non-metallic shield materials (like aluminized mylar) with a drain wire, treat the drain wire a s the shield connection as in the cases described for metallic shields.

5.4.0 LVDS SIGNAL QUALITY: JITTER MEASUREMENTS USING EYE PATTERNS

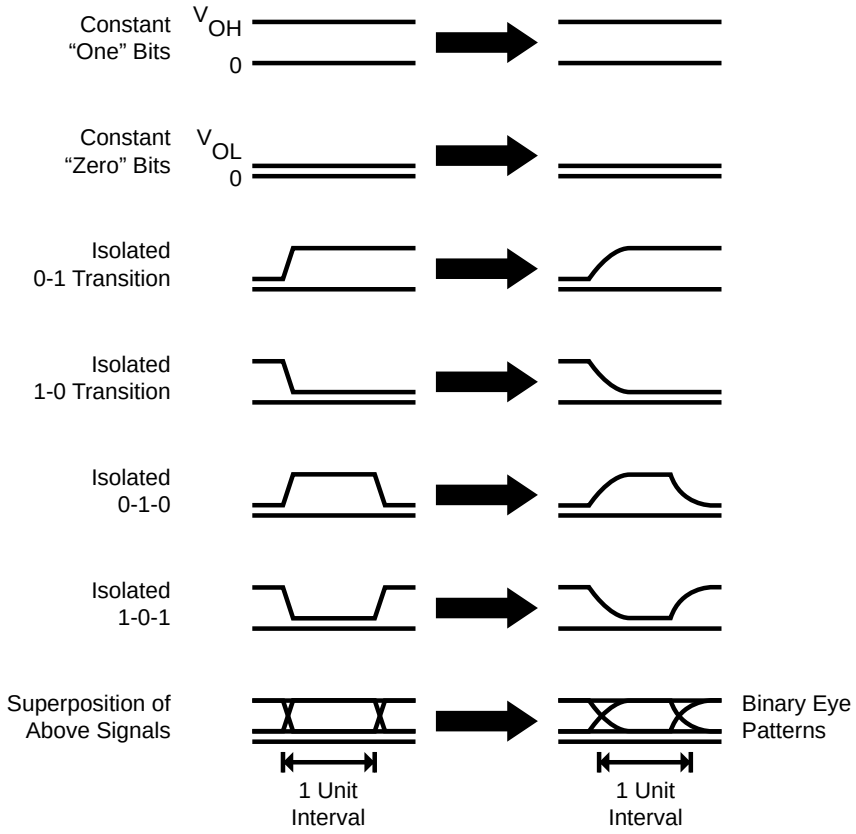
5.4.1 LVDS Signal Quality

This report provides data rate versus cable length recommendations for LVDS drivers and receivers in a typical application for a particular twisted pair cable. The questions of: "How Far?" and "How Fast?" seem simple to answer at first, but after detailed study their answers become quite complex. This is not a simple device parameter specification. But rather, a system level question where a number of other parameters besides the switching characteristics of the drivers and receivers must be known. This includes the measurement criteria for signal quality that has been selected, and also the pulse coding that will be used (NRZ for example). Additionally, other system level components should be known too. This includes details about cables, connectors, and printed circuit board (PCB). Since the purpose is to measure signal quality, it should be done in a test fixture that closely matches the end environment — or even better — in the actual application. Eye pattern measurements are useful in measuring the amount of jitter versus the unit internal to establish the data rate versus cable length curves and therefore are a very accurate way to measure the expected signal quality in the end application.

5.4.2 Why Eye Patterns?

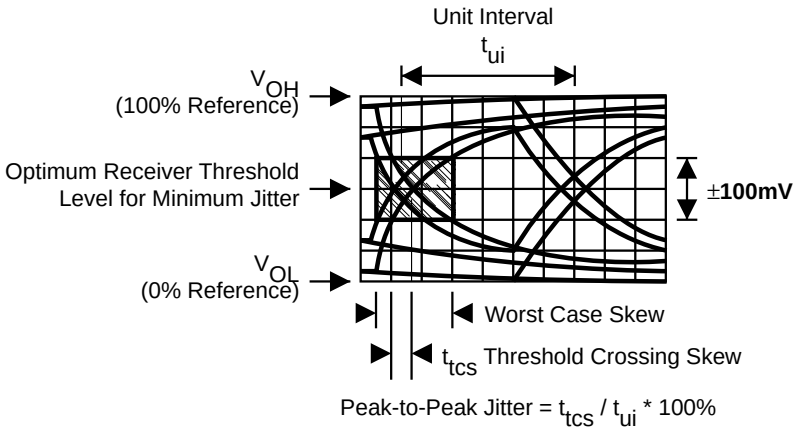
The eye pattern is used to measure the effects of inter symbol interference on random data being transmitted through a particular medium. The transition time of the signal is effected by the prior data bits. This is especially true for NRZ data which does not guarantee transitions on the line. For example in NRZ coding, a transition high after a long series of lows has a slower rise time than the rise time of a periodic (010101) waveform. This is due to the low pass filter effects that the cable causes. The figure below illustrates the superposition of six different data patterns. Overlaid they form the eye pattern that is the input to the cable. The right hand side of this figure illustrates the same pattern at the end of the cable. Note the rounding of the formerly sharp transitions. The width of the crossing point is now wider, and the opening of the eye is also now smaller (see application note AN-808 for an extensive discussion on eye patterns).

When line drivers (generators) are supplying symmetrical signals to clock leads, the period of the clock, rather than the unit interval of the clock waveform, should be used to determine the maximum cable lengths (e.g., though the clock rate is twice the data rate, the same maximum cable length limits apply). This is due to the fact that a periodic waveform is not prone to distortion from inter symbol distortion as is a data line.



Formation of an Eye Pattern by Superposition.

The figure below describes the measurement locations for minimum jitter. Peak-to-Peak Jitter is the width of the signal crossing the optimal receiver thresholds. For a differential receiver, that would correspond to 0V (differential). However, the receiver is specified to switch between –100mV and +100mV. Therefore for a worse case jitter measurement, a box should be drawn between ±100mV and jitter measured between the first and last crossing at ±100mV. If the vertical axis units in the figure were 100mV/division, the worse case jitter is at ±100mV levels.



NRZ Data Eye Pattern.

5.4.3 Eye Pattern Test Circuit

LVDS drivers and receivers are intended to be primary used in an uncomplicated point-to-point configuration as shown in the figure below. This figure details the test circuit that was used to acquire the Eye pattern measurements. It includes the following components:

PCB#1: DS90C031 LVDS Quad Driver soldered to the PCB with matched PCB traces between the device (located near the edge of the PCB) to the connector. The connector is a AMP amplite 50 series connector.

Cable: Cable used for this testing was Berk-Tek part number 271211. This is a 105Ω (Differential Mode) l28 AWG stranded twisted pair cable (25 Pair with overall shield) commonly used on SCSI applications. This cable represents a common data interface cable. For this test report the following cable lengths were tested: 1, 2, 3, 5, and 10 meter(s). Cables longer that 10 meters were not tested, but may be employed at lower data rates.

PCB#2: DS90C032 LVDS Quad Receiver soldered to the PCB with matched PCB traces between the device (located near the edge of the PCB) to the connector. The connector is a AMP amplite 50 series connector. A 100Ω surface mount resistor was used to terminate the cable at the receiver input pins.

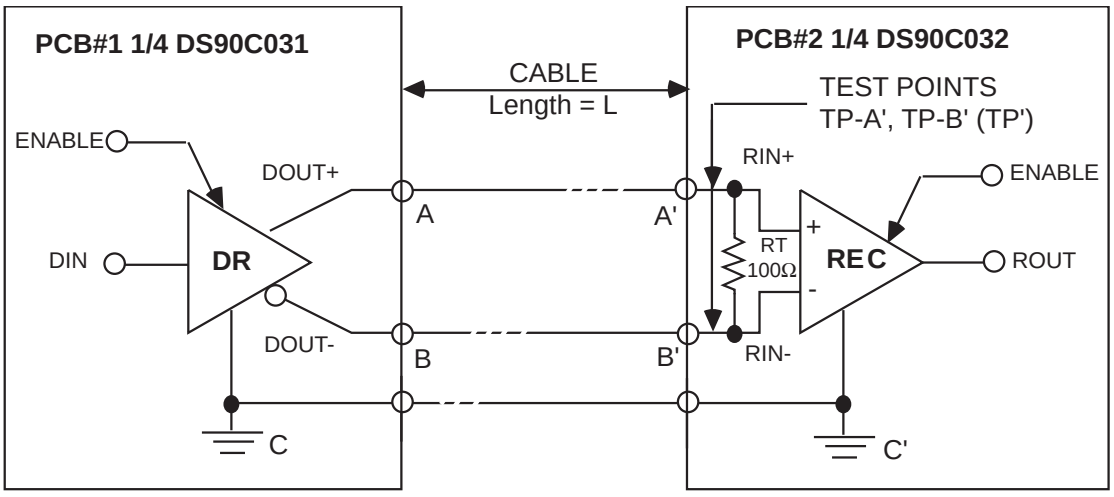


Figure 3. LVDS Signal Quality Test Circuit

5.4.4 Test Procedure

A pseudo-random (PRBS) generator was connected to the driver input, and the resulting eye pattern (measured differentially at TP') was observed on the oscilloscope. Different cable lengths (L) were tested, and the frequency of the input signal was increased until the measured jitter equaled 20% with respect to the unit interval for the particular cable length. The coding scheme used was NRZ. Jitter was measured twice at two different voltage points. First, jitter was measured at the 0V differential voltage (optimal receiver threshold point) for minimum jitter, and second at the maximum receiver threshold points (±100mV) to obtain the worst case or maximum jitter at the receiver thresholds. Occasionally jitter is measured at the crossing point alone, this will result in a much lower jitter point, but ignores the fact that the receivers may not switch at that very point. For this reason this signal quality test report measured jitter at both points.

5.4.5 Results and Data Points

20% Jitter Table @ 0V Differential (Minimum Jitter)

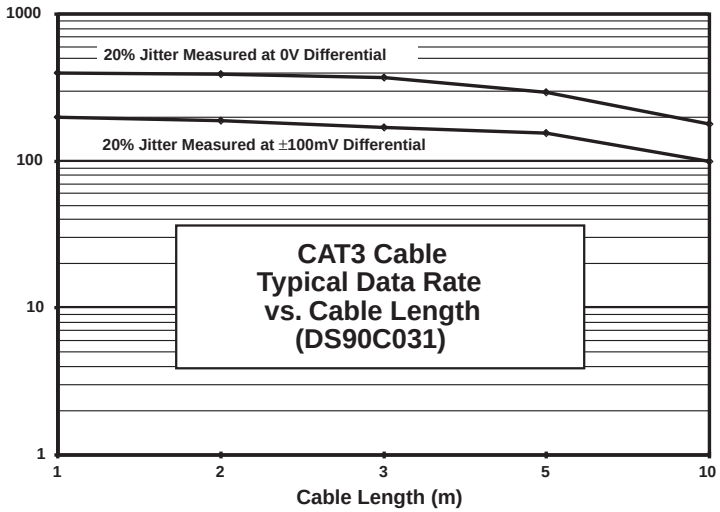
Cable Length (m)	Data Rate (Mbps)	Unit Interval (ns)	Jitter (ns)
1	400	2.500	0.490
2	391	2.555	0.520
3	370	2.703	0.524
5	295	3.390	0.680
10	180	5.550	1.160

As described above, Jitter was measured at the 0V differential point. For the case with the 1 meter cable, 490ps of jitter at 400Mbps was measured, and 1.160ns of jitter at 180Mbps and with the 10 meter cable.

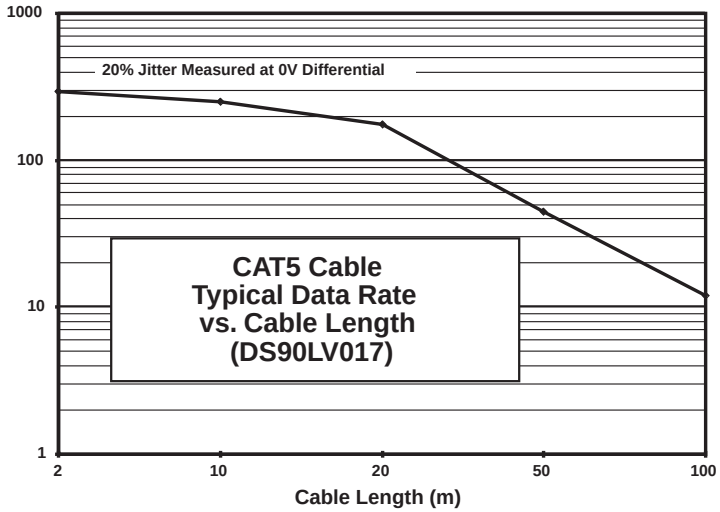
20% Jitter Table @ ±100 mV (Maximum Jitter)

Cable Length (m)	Data Rate (Mbps)	Unit Interval (ns)	Jitter (ns)
1	200	5.000	1.000
2	190	5.263	1.053
3	170	5.882	1.176
5	155.5	6.431	1.286
10	100	10.000	2.000

The second case measured jitter between ±100mV levels. For the 1 meter cable, 1ns of jitter was measured at 200Mbps, and for the 10 meter cable, 2ns of jitter occurred at 100Mbps.



Typical Data Rate vs. Cable Length for 0-10m CAT3 Cable.



Typical Data Rate taken just prior to printing this document for 2-100m CAT5 Cable

The figures above are a graphical representation of the relationship between data rate and cable length for the application under test. Both curves assume a maximum allotment of 20% jitter with respect to the unit interval. Basically, data rates between 200-400 Mbps are possible on the shorter lengths, and rates of 100-200Mbps are possible at 10 meters. Note that employing a different coding scheme, cable, wire gauge (AWG), etc. will create a different relationship between maximum data rate versus cable length. Designers are greatly encouraged to experiment on their own.

5.4.6 Conclusions

Eye patterns provide a useful tool to analyze jitter and the resulting signal quality as it captures the effects of a random data pattern. They provide a method to determine the maximum cable length for a given data rate or vice versa. Different systems, however, can tolerate different levels of jitter. Commonly 5%, 10%, or 20% is acceptable with 20% jitter usually being an upper practical limit. More than 20% jitter tends to close down the eye opening, making error-free recovery of NRZ data more difficult. This report illustrates data rate versus distance for a common, inexpensive type of cable.

5.5.0 BIT ERROR RATE (BER) TESTING

5.5.1 LVDS Cable Driving Performance

The questions of: “How Far?” and “How Fast?” seem simple to answer at first, but after detailed study their answers become quite complex. This is not a simple device parameter specification. But rather, a system level question, and to be answered correctly a number of other parameters besides the switching characteristics of the drivers and receivers must be known. This includes the measurement criteria for signal quality that has been selected, and the pulse coding that will be used (Non-Return to Zero (NRZ) for example — see application note AN-808 for more information about coding). Additionally, other system level components should be known too. This includes details about the cable, connector, and information about the printed circuit board (PCB). Since the purpose is to measure signal quality/performance, it should be done in a test fixture that matches the end environment precisely if possible. The actual application would be best if possible. There are numerous methods to measure signal quality, including eye pattern (jitter) measurements and Bit Error Rate tests (BER).

This report provides the results of a series of Bit Error Rate tests performed on the DS90C031/2 LVDS Quad Line Driver/Receiver devices. The results can be generalized to other National LVDS products. Four drivers were used to drive 1 to 5 meters of standard twisted pair cables at selected data rates. Four receivers were used to recover the data at the load end of the cable.

5.5.2 What is a BER Test?

Bit Error Rate testing is one way to measure of the performance of a communications system. The standard equation for an bit error rate measurement is:

Bit Error Rate = (Number of Bit errors) / (Total Number of Bits)

Common measurement points are bit error rates of:

$<1 \times 10^{-12}$ => One or less errors in 1 trillion bits sent

$<1 \times 10^{-14}$ => One or less errors in 100 trillion bits sent

Note that BER testing is time intensive. The time length of the test is determined by the data rate and also the desired performance bench mark. For example if the data rate is 50Mbps, and the bench mark is an error rate of 1×10^{-14} or better, a run time of 2,000,000 seconds is required for a serial channel. 2,000,000 seconds equates to 555.6 hours or 23.15 days!

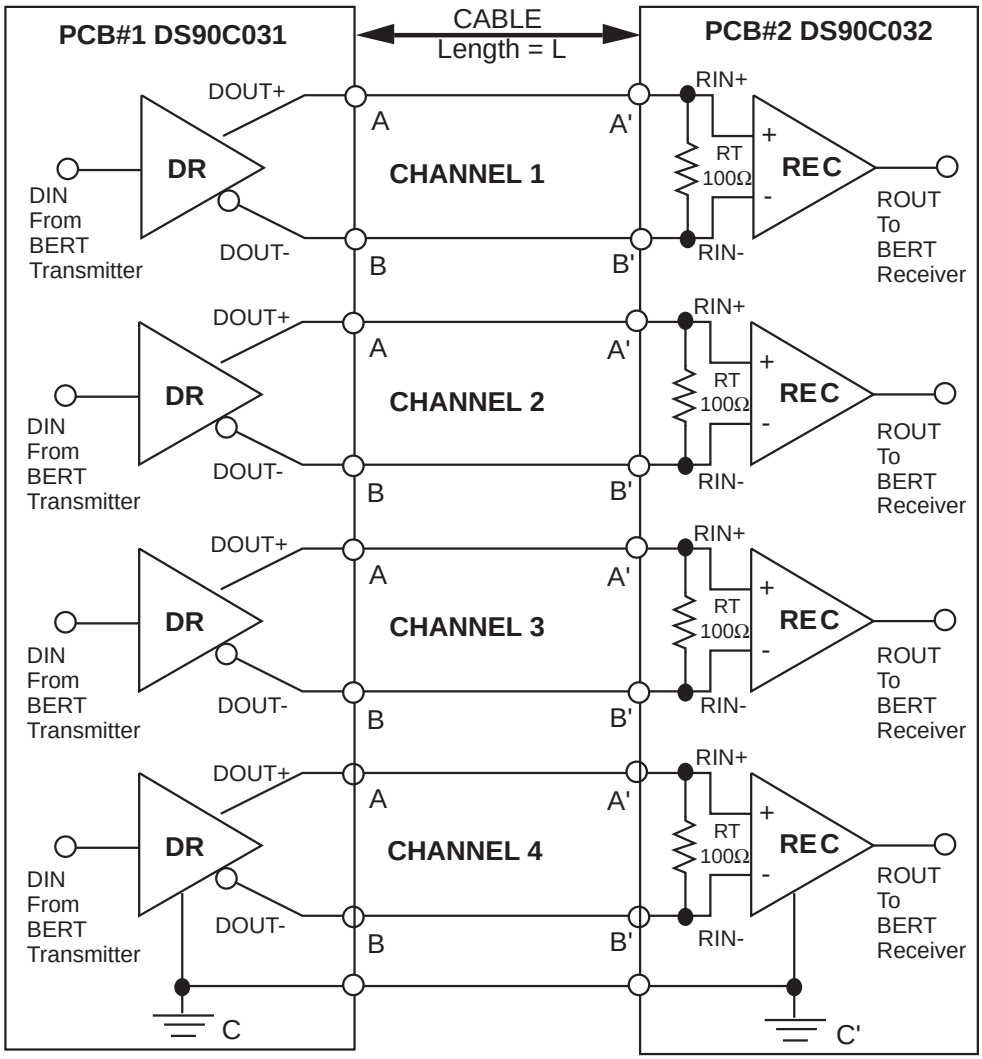
5.5.3 BER Test Circuit

LVDS drivers and receivers are intended to be primary used in an uncomplicated point-to-point configuration as shown in Figure 1. This figure details the test circuit that was used. It includes the following components:

PCB#1: DS90C031 LVDS Quad Driver soldered to the PCB with matched PCB traces between the device (located near the edge of the PCB) to the connector. The connector is an AMP amplite 50 series connector

Cable: Cable used for this testing was Berk-Tek part number 271211. This is a 105Ω (Differential Mode) 28 AWG stranded twisted pair cable (25 Pair with overall shied) commonly used in SCSI applications. This cable represents a common data interface cable. For this test report cable lengths of 1 and 5 meters were tested.

PCB#2: DS90C032 LVDS Quad Receiver soldered to the PCB with matched PCB traces between the device (located near the edge of the PCB) to the connector. The connector is a AMP amplite 50 series connector. A 100Ω surface mount resistor was used to terminate the cable at the receiver input pins.



LVDS BER test circuit.

5.5.4 Test Procedure

A parallel high-speed BER transmitter/receiver set (Tektronix MultiBERT-100) was employed for the tests. The transmitter was connected to the driver inputs, and the receiver outputs were connected to the BERT receiver inputs. Different cable lengths and data rates were tested. The BER tester was configured to provide a PRBS (Pseudo Random Bit Sequence) of 2^{15}-1 (32,767 bit long sequence). In the first test, the same input signal was applied to all four of the LVDS channels under test. For the other tests, the PRBS was offset by 4 bits, thus providing a random sequence between channels. The coding scheme used was NRZ. Upon system test configuration, the test was allowed to run uninterrupted for a set amount of time. At completion of the time block the results were recorded which included: elapsed seconds, total bits transmitted, and number of bit errors recorded. For the three tests documented below, a power supply voltage of +5.0V was used, and the tests were conducted at room temperature.

5.5.5 Tests and Results

The goal of the tests was to demonstrate errors rates of less than <1 x 10-12 are obtainable.

TEST #1 Conditions:
- Data Rate = 50Mbps
- Cable Length = 1 meter
- PRBS Code = 2^{15}-1 NRZ

For this test, the PRBS code applied to the four driver inputs was identical. This created a "simultaneous output switching" condition on the device.

TEST #1 Results:
- Total Seconds: 87,085 (1 day)
- Total Bits: 1,723 x 1013
- Errors = 0
- Error Rate = < 1 x 10^{-12}

TEST #2 Conditions:
- Data Rate = 100Mbps
- Cable Length = 1 meter
- PRBS Code = 2^{15}-1 NRZ

For this test, the PRBS code applied to the four driver inputs was offset by four bits. This creates a random pattern between channels.

TEST #2 Results:
- Total Seconds: 10,717 (~3 hr.)
- Total Bits: 4.38 x 1012
- Errors = 0
- Error Rate = < 1 x 10^{-12}

TEST #3 Conditions:
- Data Rate = 100Mbps
- Cable Length = 5 meter
- PRBS Code = 2^{15}-1 NRZ

For this test, the PRBS code applied to the four driver inputs was offset by four bits. This creates a random pattern between channels.

TEST #3 Results:
- Total Seconds: 10,050
- Total Bits: 4 x 1012
- Errors = 0
- Error Rate = < 1 x 10^{-12}

5.5.6 Conclusions

All three of the tests ran error free and demonstrate extremely low bit error rates using LVDS technology. The tests concluded error rates of < 1 x 10^{-12} can be obtained at 100Mbps operation across 5 meters of twisted pair cable. BER tests only provide a "Go — No Go" data point if zero errors are detected. It is recommended to conduct further tests to determine the point of failure (data errors). This will yield important data that indicates the amount of margin in the system. This was done in the tests conducted by increasing the cable length from 1 meter to 5 meters, and also adjusting the data rate from 50Mbps to 100Mbps. Additionally, bench checks were made while adjusting the power supply voltage from 5.0V to 4.5V and 5.5V, adjusting clock frequency, and by applying heat/cold to the device under test (DUT). No errors were detected during these checks (tests were checks only and were not conducted over time, i.e. 24 hours). BER tests conclude that the PRBS patterns were transmitted error free across the link. This was concluded by applying a pattern to the input and monitoring the receiver output signal.

LVDS Evaluation Boards

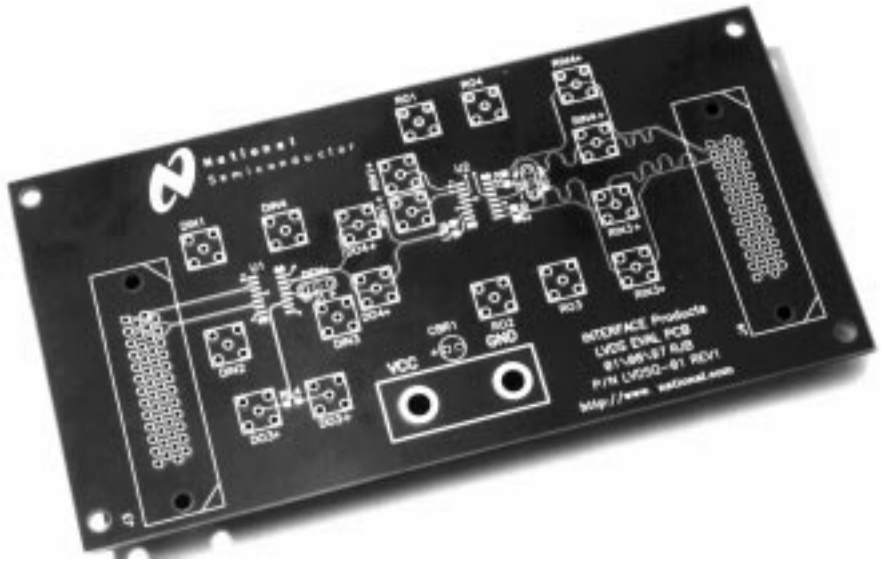
Chapter 6

6.0.0 LVDS EVALUATION BOARDS

Presently there are two types of evaluation boards available: The high speed link (includes Channel Link and FPD-Link) evaluation boards and the Generic LVDS Evaluation Board. (See the selection tables in chapter 3 for a cross reference list of boards versus devices.) The high speed link evaluation boards can be ordered through National's distributors and come complete with a transmitter board, receiver board, ribbon cable, instructions, and datasheets.

FPD-Link Evaluation Board (the Channel Link evaluation board is similar)

These boards are fully populated. TTL signals are accessed through a 50-pin IDC connector on the transmitter and receiver boards. The boards are interconnected via a ribbon cable that can be modified for custom lengths. These evaluation boards are useful for analyzing the operation of National's high speed Channel Link and FPD-Link devices in your system. For LVDS signal quality measurements over other interconnect media, use the Generic LVDS evaluation board.



The Generic LVDS Evaluation Board

The Generic LVDS Evaluation Board is used to measure LVDS signaling performance over different media. Individual LVDS channels can be evaluated over PCB trace, twisted pair cable, or custom transmission medium. Though LVDS quad drivers and receivers are used on the board, they can represent the LVDS I/O characteristics of most of National's LVDS devices.

a) Use the DS90C031/032 to represent the LVDS I/O characteristics of all 5V drivers/receivers, 5V Channel Link, and 5V FPD-Link devices.

b) Use the DS90LV031/032 to represent the LVDS I/O characteristics of the DS90LV031/032/017/027 devices.

c) Use the upcoming DS90LV031A/032A (available in October 1997) to represent the LVDS I/O characteristics of 3V Channel Link, 3V FPD-Link, and other 3V devices not listed in (b) above.

The remainder of this chapter is devoted to explaining the operation of the Generic LVDS Evaluation board.

6.1.0 THE GENERIC LVDS EVALUATION BOARD

6.1.1 Purpose

The purpose of the Low Voltage Differential Signaling (LVDS) Evaluation Printed Circuit Board (PCB) is to demonstrate the line driving capability of LVDS technology across a short PCB interconnect, and also across a variable length of twisted pair cable. Probe points for a separate driver and a separate receiver are also provided for individual line driver or receiver testing. The part number for the Evaluation PCB is LVDSEVAL-001 (stuffed) or Literature number 550061-001 (unstuffed - limit one per Customer, while supplies last). In this application note and on the PCB the following differential signal nomenclature has been used: "A" represents the true signal and "B" represents the inverting signal. Driver input signals are represented with an "I" while receiver outputs are with an "O."

6.1.2 Five Test Cases

Five different test cases are provided on this simple 4 layer FR-4 PCB. Each case is described separately next. Note that the driver / receiver numbers do not directly map to the LVDS test channel number (LVDS Channel 1 utilizes driver number 1 and receiver number 4). The five test cases are shown in figure 1.

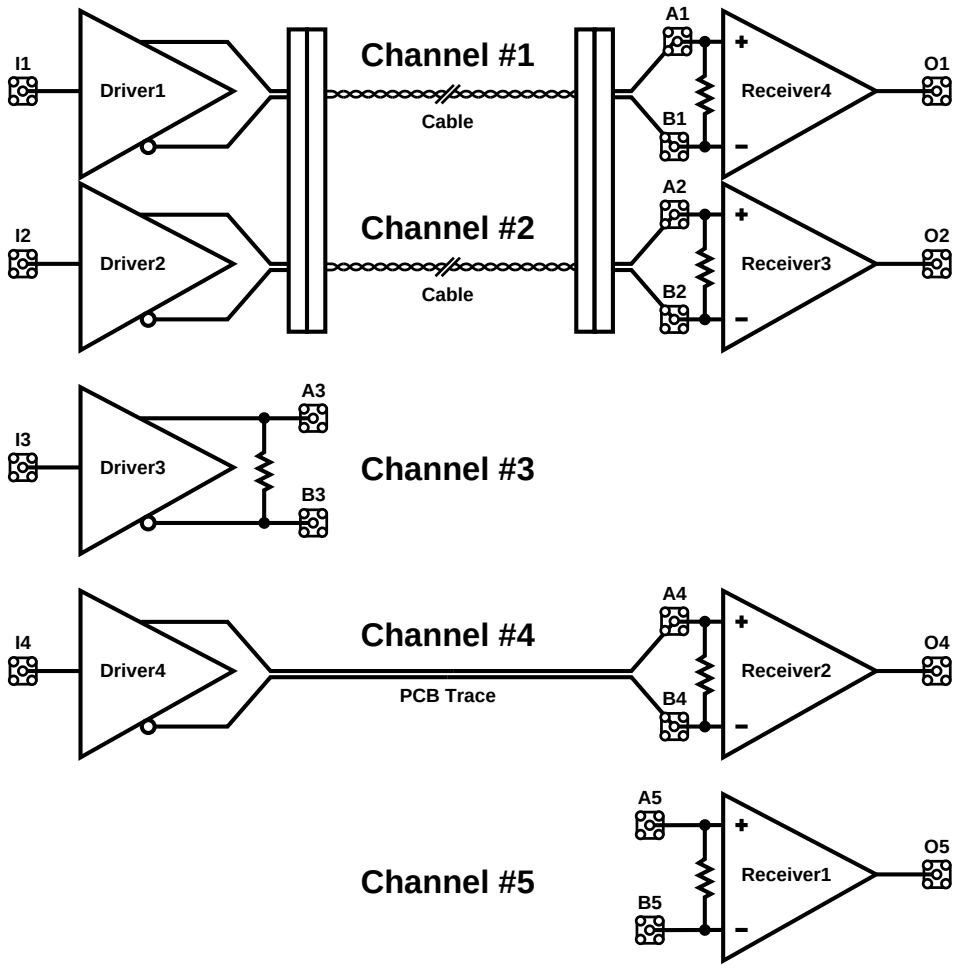


Figure 1: PCB Block Diagram

LVDS Channel # 1: Cable Interconnect

This test channel connects Driver #1 to Receiver #4 via the cable interconnect. A SMB test point interface is provided at the receiver input side of the cable. The driver input signal (I1) is terminated with a 50 Ohm termination resistor on the bottom side of the PCB. LVDS signals are probed via test points A1 and B1. The receiver output signal may be probed at test point O1. A PCB option for a series 450 Ohm resistor is also provided in case 50 Ohm probes are employed on the receiver output signal (see options section). A direct probe connection is possible with a high impedance probe (>100 k Ohm loading) on the LVDS signals at test points A1 and B1.

LVDS Channel # 2: Cable Interconnect

This test channel connects Driver #2 to Receiver #3 also via the cable interconnect. A SMB test point interface is provided at the receiver input side of the cable. The driver input signal (I2) is terminated with a 50 Ohm termination resistor on the bottom side of the PCB. LVDS signals are probed via test points A2 and B2. The receiver output signal may be probed at test point O2. A PCB option for a series 450 Ohm resistor is also provided in case 50 Ohm probes are employed on the receiver output signal. A direct probe connection is possible with a high impedance probe (>100 k Ohm loading) on the LVDS signals at test points A2 and B2. This channel duplicates channel #1 so that it may be used for a clock function or for cable crosstalk measurements.

LVDS Channel # 3: LVDS Line Driver

This test channel provides test points for an isolated driver with a standard 100 Ohm differential termination load. Probe access for the driver outputs is provided at test points A3 and B3. The driver input signal (I3) is terminated with a 50 Ohm termination resistor on the bottom side of the PCB.

LVDS Channel # 4: PCB Interconnect

This test channel connects Driver #4 to Receiver #2 via a pure PCB interconnect. A SMB test point interface of the LVDS signaling is provided at test points A4 and B4. The driver input signal (I4) is terminated with a 50 Ohm termination resistor on the bottom side of the PCB. The receiver output signal may be probed at test point O4. A PCB option for a series 450 Ohm resistor is also provided in case 50 Ohm probes are employed on the receiver output signal. A direct probe connection is possible with a high impedance probe (>100 k Ohm loading) on the LVDS signals at test points A4 and B4. This channel may be used for analyzing the LVDS signal without the bandwidth limiting effects of a cable interconnect.

LVDS Channel # 5: LVDS Receiver

This test channel provides test points for an isolated receiver. Termination options on the receiver inputs accommodate either a 100 Ohm resistor connected across the inputs (differential) or two separate 50 Ohm terminations (each line to ground). The second option allows for a standard signal generator interface. Input signals are connected at test points A5 and B5. A PCB option for a series 450 Ohm resistor is also provided in case 50 Ohm probes are employed on the receiver output signal. The receiver output signal may be probed at test point O5.

6.1.3 Interconnecting Cable and Connector

The evaluation PCB has been designed to directly accommodate a 25 pair (50-pin) SCSI-2 cable commonly referred to as an “A” cable. The pinout, connector, and cable electrical/mechanical characteristics are defined in the SCSI-2 standard and the cable is widely available. The connector is 50 position, with 0.050 centers and the pairs are pinned out up and down. For example pair 1 is on pins 1 and 26, not pins 1 and 2.

IMPORTANT NOTE: The 23 unused pairs and the overall shield are connected to ground. Other cables may also be used if they are built up.

6.1.4 PCB Design

Due to the high speed switching rates obtainable by LVDS a minimum of a four layer PCB construction and FR-4 material is recommended. This allows for 2 signal layers and full power and ground planes. The stack is: signal (LVDS), ground, power, signal (TTL/CMOS).

Differential traces are highly recommended for the driver outputs and the receiver inputs signal (LVDS signals, see PCB layout between U1 and J3). Employing differential traces will ensure a low emission design and maximum common mode rejection of any coupled noise. Differential traces require that the spacing between the differential pair be controlled. This distance should be held as small as possible to ensure that any noise coupled onto the lines will primarily be common mode. Also by keeping the pair close together the maximum canceling of fields is obtained. Differential impedance of the trace pair should be matched to the selected interconnect media (cable’s differential characteristic impedance). Equations for calculating differential impedance are contained in chapter 4 of the LVDS Owner’s Manual and also in National application note AN-905 for both microstrip and stripline differential PCB traces.

Termination of LVDS lines is required to complete the current loop and for the drivers to properly operate. This termination in its simplest form is a single surface mount resistor (surface mount resistor minimizes parasitic elements) connected across the differential pair as close to the receiver inputs as possible (should be within 0.5 inch (13 mm) of input pins). Its value should be selected to match the interconnects differential characteristics impedance. The closer the match the higher the signal fidelity and the less common mode reflections will occur (lower emissions too). Typical values are 100 or 121 Ohm ±5% (media specific).

LVDS signals should be kept away from CMOS logic signals to minimize noise coupling from the large swing CMOS signals. This has been accomplished on the PCB by routing CMOS signals on a different signal layer (bottom) than the LVDS signals (top) wherever possible. If they are required on the same layer, a CMOS signal should never be routed within three times (3S) the distance between the differential pair (S). Adjacent differential pairs should be at least 2S away also.

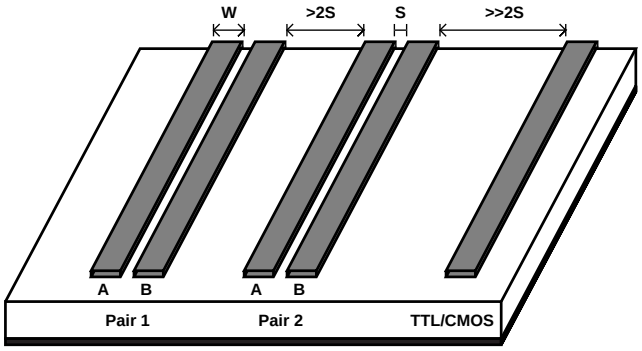


Figure 2: Pair Spacing for differential lines

Bypassing capacitors are recommended for each package. 0.1 µF is sufficient on the quad driver or receiver device (CB2 and CB3) however, additional smaller value capacitors may be added (i.e. 0.001 µF at CB12 and CB13) if desired. Traces connecting Vcc and ground should be wide (low impedance, not 50 Ohm dimensions) and employ multiple vias to reduce inductance. Bulk bypassing is provided (CBR1, close by) at the main power connection as well. Additional power supply high frequency bypassing can be added at CB1, CB11, and CB21 if desired.

6.1.5 Sample Waveforms from the LVDS Evaluation PCB

Single-ended signals are measured from each signal (true and inverting signals) with respect to ground. The receiver ideally switches at the crossing point of the two signals. LVDS signals should swing between 1.0 V (V_{OL}) and 1.3 V (V_{OH}) for a 300 mV V_{OD}. The differential waveform is constructed by subtracting the B (inverting) signal from the A (true) signal. V_{OD} = A - B. The V_{OD} magnitude is either positive or negative, so the differential swing (V_{SS}) is twice the V_{OD} magnitude. Drawn single-ended waveforms and the corresponding differential waveforms are shown in Figure #3.

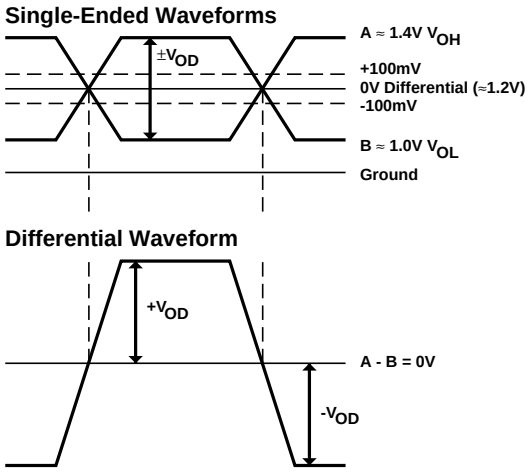


Figure 3: Single-ended & Differential Waveforms

The PCB interconnect signal (LVDS Channel #4) can be measured at the receiver inputs (test points A4 and B4). Due to the short interconnect path via the PCB little distortion to the waveform is caused by the interconnect. See figure 4. Note that the data rate is 50 Mbps and the differential waveform (V_{DIFF}) shows fast transition times with little distortion.

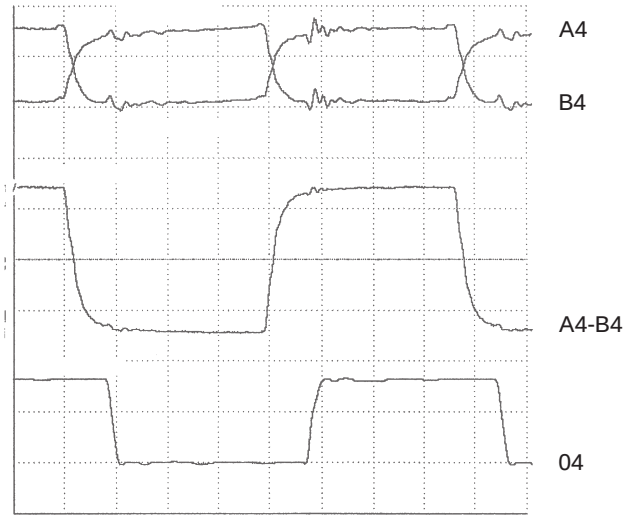


Figure 4: LVDS Channel #4 Waveforms — PCB Interconnect

The cable interconnect signal is also measured at the receiver inputs (test points A1 & B1 and A2 & B2). Due to the characteristics of the cable some waveform distortion has occurred. Depending upon the cable length and quality, the transition time of the signal at the end of the cable will be slower than the signal at the driver's outputs. This effect can be measured by taking rise and fall measurements and increasing the cable length. A ratio of transition time to unit interval (minimum bit width) is a common gauge of signal quality. Depending upon the application ratios of 30% to 50% are common. These measurements tend to be more conservative than jitter measurements. The waveforms acquired with a SCSI-2 cable of 1 meter and also 2 meters in length are shown in figure 5 and 6. Note the additional transition time slowing due to the cable's filter effects on the 2 meter test case.

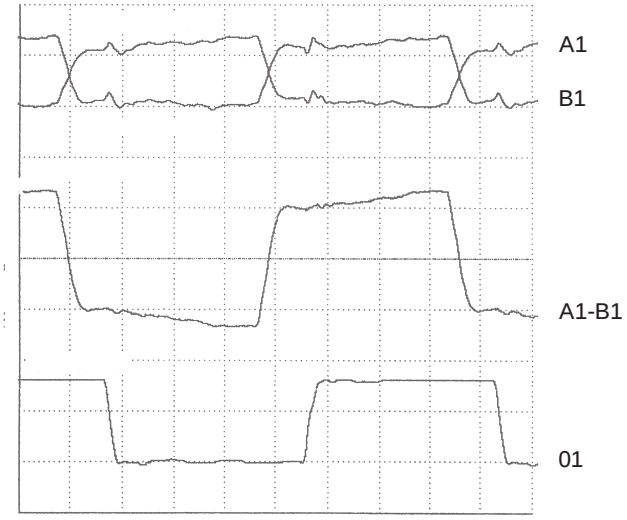


Figure 5: LVDS Channel #1 Waveforms - 1m Cable Interconnect

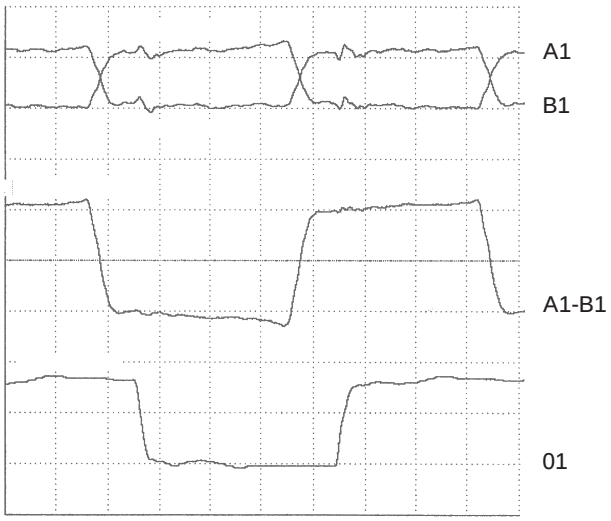


Figure 6: LVDS Channel #1 Waveforms - 2m Cable Interconnect

6.1.6 Probing of High Speed LVDS Signals

Probe specifications for measuring LVDS signals are unique due to the low drive level of LVDS (3 mA typical). A high impedance probe must be used (100k Ohm or greater). The capacitive loading of the probe should be kept in the low pF range, and the bandwidth of the probe should be at least 1 Ghz (4 Ghz preferred) to accurately acquire the waveform under measurement.

National's Interface Applications group employs a wide range of probes and oscilloscopes. One system that meets the requirements of LVDS particularly well is a TEK 11801B scope (50 Ghz Bandwidth) and SD14 probe heads. These probes offer 100k Ohm, 0.4 pF loading and a bandwidth of 4 Ghz. This test equipment was used to acquire the waveforms shown in figures 4, 5 and 6.

LVDS waveforms may also be measured with lower bandwidth / different loading probes such as common TEK probes P6135A (150 MHz/1M Ohm / 10.5 pF). These probes were connected to a TEK 602 scope. See figure 7 for the LVDS waveforms acquired in this set up and compare these to figure 5. The waveform shows less DC loading (1M Ohm compared to 100k Ohm) and also more capacitive loading and bandwidth limiting. Probes with standard 50 Ohm loading should not be since they will load the LVDS signals too heavily. 50 Ohm probes may be used on the receiver output signal in conjunction the 450 Ohm series resistor option (see option section below). Note that the scope waveform is an attenuated signal (50/(450 +50) or 1/10) of the output signal and the receiver output is loaded with 500 Ohm to ground.

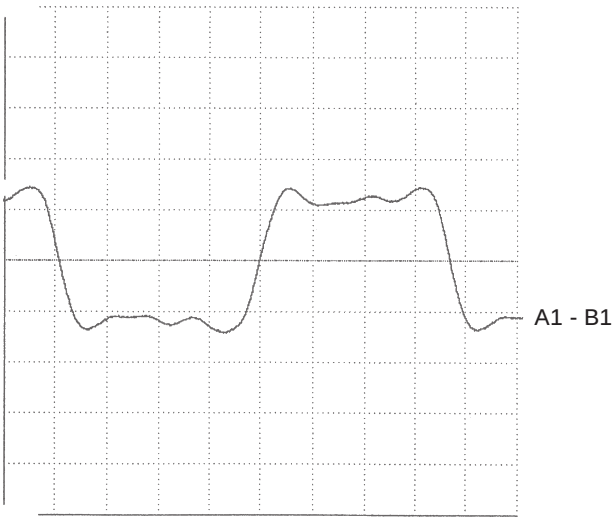


Figure 7: LVDS differential waveform measured with TEK P6135A probes and 602 scope

6.1.7 Demo PCB Options

Option 1: 450 Ohm Resistors

A provision for a series 450 Ohm resistor (RS1-4) is provided on the receiver output signal. By cutting the trace between the "RS" pads and installing a 450 Ohm resistor a standard 50 Ohm scope probe may be used (500 Ohm total load). Note that the signal is divided down (1/10) at the scope input.

Option 2: Disabling the LVDS Driver

The quad driver features a ganged enable. An active high or an active low input are provided. On the evaluation PCB the active high input has been hard wired to ground (-, off). The active low input (EN*) is routed to a jumper (J1). The jumper provides a connection to the Vcc plane (+) or to the Ground plane (-). To enable the driver connect the jumper to ground, to disable the driver connect the jumper to the power plane.

Option 3: Disabling the LVDS Receiver

The quad receiver features a ganged enable (same as the driver). An active high or an active low are provided. On the evaluation PCB the active high input has been hard wired to ground (-, off). The active low input (EN*) is routed to a jumper (J2). The jumper provides a connection to the Vcc plane (+) or to the Ground plane (-). To enable the receiver connect the jumper to ground, to disable the receiver connect the jumper to the power plane.

Option 4: Cables

Different cables may also be tested (different lengths, materials, constructions). A standard SCSI-2 50-pin connector/pinout has been used (J3 and J4). Simply plug in a SCSI-2 cable or build a custom cable.

Option 5: Power Supply /Components (C/LV/422)

The LVDS quads are offered in an industry standard pinout made popular by the 26LS31/2 quad 5V RS-422 devices. This standard pinout allows different devices (and power supplies) to be substituted and evaluated. The following National Semiconductor devices may be tested (U1/U2):

Devices (D/R)	Power Supply	Signaling Levels
DS90C031/2	5V	LVDS Signals
DS90LV031/2	3.3V	LVDS Signals
DS90LV031A/2A	3.3V	FAST LVDS (planned devices)
DS26C31/2A	5V	RS-422 Signals
DS26LV31/2A	3.3V	RS-422 Signals

Option 6: Receiver Termination (Channel #5)

The separate receiver input signals can be terminated separately (50 Ohm on each line to ground) utilizing pads RT5 (true input to ground) and RT6 (inverting to ground) for a signal generator interface. Or with a single 100 Ohm differential resistor (pad RL5) if the device is to be driven by a differential driver.

6.1.8 Plug & Play

The following simple steps should be taken to begin testing on your completed evaluation board:

1) Connect signal common (Ground) to the black binding post

2) Connect the power supply lead to the red binding post (5V or 3.3V)

3) Set J1 & J2 jumpers to ground (-) to enable the drivers and receivers

4) Connect a signal generator to the driver input (I4) with:

a) frequency = 50 Mhz (100 Mbps)

b) V_{IL} = 0V & V_{IH} = 3.0V

c) t_r & t_f = 2 ns

d) duty cycle = 50% (square wave)

5) Connect high impedance probes to test points A4 and B4

6) View LVDS signals using the same voltage offset and volts/div settings on the scope with high impedance probes. View the output signal on a separate channel from test point O4.

6.1.9 Common Mode Noise

When the receivers (DS90C032, DS90LV032) are enabled common mode noise is passed from the output of the receiver to the inputs. This noise shows up on the single-ended waveforms, but does not impact the differential waveform that carries the data. For improved signal fidelity a design improvement is under way to reduce the magnitude of the noise coupled back to the inputs. This noise will not be observed if the receiver device is disabled by setting J2 to “+”.

6.1.10 Summary

This evaluation PCB provides a simple tool to evaluate LVDS signaling across different media and lengths to determine signal quality for data transmission applications.

6.1.11 Appendix

Typical test equipment used for LVDS measurements:

Signal Generator	TEK HFS 9009
Oscilloscope	TEK 11801B
Probes	TEK SD-14

Bill of Materials

Type	Label	Value / Tolerance	Qty	Footprint	Part Number
IC	U1	(Quad Driver)	1	16-L SOIC	DS90LV031TM or other
IC	U2	(Quad Receiver)	1	16-L SOIC	DS90LV032TM or other
Connector	J3, J4	(50 pin SCSI-2)	2		AMP P/N 749721-5
Resistor	RT1-4	50 Ohm	4	RC0805	
Resistor	RL1-5	100 Ohm	5-Apr	RC0805	
Resistor	RS1-4	450 Ohm	0/4	RC0805	
Capacitor	CB2, CB3	0.1 uF	2	CC0805	
Capacitor	CB12, CB13	0.001 uF	0/2	CC0805	
Capacitor	CBR1	10 uF, 16V	1	CAP100RP	Electrolytic Radial Lead
Capacitor	CB1/11/21	na	0/3	CC0805	
Jumper Stakes	J1, J2x	3 STAKES	2		100 mil spacing
Jumpers	-		2		
SMB Jack	-		18	SMB Connector	Labels: I1-4, A1-5, B1-5, O1-2, O4-5. EF Johnson P/N 131-1701-201
Plug		Binding Post	2		Superior Electronic P/N BP21R, BP21B (1 each)
Cable	na	SCSI-2 type A Cable	0/1		
Legs			4		
bolts/washers			4		
PCB			1		LVDSEVAL-001 or LIT#550061-001

Reference and Fax Feedback Form

Chapter 7

7.0.0 REFERENCE AND CONTACT INFORMATION

7.1.0 APPLICATION NOTES

The list of additional application information about LVDS is growing. Following is a list of application notes at press time. The 1996 Interface Databook (literature number 400045) contains much information, but is now outdated. Up-to-date information can be retrieved from our Website.

	AN#	Title	Databook[1]	Web[2]
LVDS	AN-971	An Overview of LVDS Technology	•	•
	AN-977	LVDS Signal Quality: Jitter Measurements Using Eye Pattern	•	•
	AN-1035	PCB Design Guidelines for LVDS Technology	•	•
	AN-1040	Bit Error Rate (BER) Testing Data		•
	AN-1060	EDN Article Reprint (1/97)		•
Channel & FPD Links	AN-1032	An Introduction to FPD Link	•	•
	AN-1041	Channel Link Introduction		•
	AN-1045	FPD Rising/Falling Edge Clocking and Bit Mapping		•
	AN-1056	FPD STN Panel Applications		
	AN-1059	Skew and Jitter		
General	AN-806	Data Transmissions Lines and Their Characteristics	•	•
	AN-807	Reflections:Computations & Waveforms	•	•
	AN-808	Long Transmission Lines & Data Signal Quality	•	•
	AN-905	Transmission Line Rapidesigner Operations[3]		•
	AN-912	Common Data Transmission Parameters & Their Definitions	•	•
	AN-916	A Practical Guide To Cable Selection	•	•
	Sect. 13	IBIS Simulation Model Information	•	

[1]The literature number for the Interface Databook is Lit# 400045

[2] National's Web address is http://www.national.com

[3] The literature number for the Transmission Line Rapidesigner is Lit# 633200-001 (metric) or 633201-001 (English units). (The accompanying application note, AN-905, is also available separately as Lit# 100905-001)

7.2.0 ANSI/TIA/EIA-644 STANDARD

To order copies of the ANSI/TIA/EIA-644 Standard contact:

Global Engineering Documents
15 Inverness Way East
Englewood, CO 80112-5704

or call

USA and Canada: 1.800.854.7179
International: 1.303.397.7956

7.3.0 IBIS I/O MODEL INFORMATION

I/O Buffer Information Specification (IBIS) is a behavioral model specification defined within the ANSI/EIA-656 standard. LVDS IBIS models are available from National's Website which can be used by almost any simulators/EDA tools in the industry.

Visit the ANSI/EIA-656 Website: **www.eia.org/EIG/IBIS/ibis.htm** for a vendor listing or contact your software vendor. Chapter 13 of National's 1996 Interface Databook (lit#400045) describes IBIS models in detail.

Two sets of IBIS models (DS90C031/032 and DS90LV031/032) can represent the LVDS I/O characteristics of most of National's LVDS devices.

a) Use the DS90C031/032 models to represent the LVDS I/O characteristics of all 5V drivers/receivers, 5V Channel Link, and 5V FPD-Link devices.

b) Use the DS90LV031/032 models to represent the LVDS I/O characteristics of the DS90LV031/032/017/027 devices.

c) Use the DS36C200 model for the DS36C200.

d) Contact National for availability of models to represent the LVDS I/O characteristics of 3V Channel Link, 3V FPD-Link, and other 3V devices not listed in (b) above.

National IBIS models are available at: **www.national.com/models/ibis/ibis.html**

LVDS Fax Feedback

To: **National Semiconductor LVDS Marketing**

Fax: **1.408.737.7218**

From:

Mr./Ms.	Last Name	First Name	Title
Company		Dept./Division	
Address		Mail Stop	
City		State	Zip/Country
Phone	Ext.	Fax	
Email address			

The LVDS Owner's Manual Design Guide is (check one):

❑ Excellent ❑ Good ❑ Average ❑ Poor

Comments and suggestions for improvement:

_____
_____
_____
_____

I am interested in the following LVDS products (check all that apply):

❑ Drivers/Receivers ❑ Channel Link ❑ FPD-Link ❑ Other

New product suggestions:

_____
_____
_____
_____

My application is: _____

Please call me regarding LVDS in my application (check one): ❑ Yes ❑ No

Other comments:

_____
_____
_____
_____
_____

Thank you for your feedback, it is important to us!

Index & Worldwide Sales Offices

Chapter 8